APPLICATION NOTE

OM5729
Zero-IF Digital Satellite-TV Receiver Demo Board

AN99018

Philips
Semiconductors

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Abstract

The OM5729 demo board features the PHILIPS TDA8060TS QPSK Zero-IF down converter IC, the TSA5059T Low Phase Noise I^2C-controlled Synthesizer IC and TDA8083H Satellite Demodulator and Decoder IC and is targetted for medium / high symbol rates.
This report describes the use of and the measurements on the OM5729 (pcb nr.: PR39233).
Together with the DBUI software, this demo board can be evaluated in a set-top box like environment.

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Zero-IF Digital Satellite-TV Receiver
Demo Board

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Summary

This Application note describes the TDA8060TS QPSK Zero-IF down converter IC, the TSA5059T low phase noise synthesizer IC and the TDA8083H Satellite Demodulator and Decoder IC (SDD) in the OM5729 application. The TDA8060TS is the main part of a Zero-IF satellite tuner. Together with a BFG425W Low Noise Amplifier (LNA), a pin diode attenuator and a TSA5059T low phase noise synthesizer the board acts as a nearly complete satellite tuner. This report describes the use of and the measurements on the OM5729.
The TDA8083H is intended for the reception of variable symbol rate DVB compliant MPEG2 signals, transmitted via satellite. In combination with the Zero-IF tuner part, all functions are available to deliver a corrected transport stream given an DVB encoded BPSK/QPSK signal.

CONTENTS

1. INTRODUCTION

This Application note describes the TDA8060TS QPSK Zero-IF down converter IC, the TSA5059T low phase noise synthesizer IC and partly the TDA8083H Satellite Demodulator and Decoder IC (SDD) in the OM5729 application. The OM5729 demo board can be split into two parts, the tuner part and the channel decoder part.

- ***Tuner part:***
  The tuner part contains a PHILIPS TDA8060 Zero IF QPSK down converter type for satellite tuners and a TSA5059 low phase noise Synthesizer IC.
  Via a Low Noise Block Converter (LNB), a QPSK modulated RF input signal from a satellite is fed to the 50 Ohm SMA input connector of the OM5729. The signal is then fed via an input matching network (featuring an LNB supply input pin) to an LNA with a NPN wideband transistor (BFG425W) and a PIN diode attenuator (BA595) to increase the total AGC range of the system.
  This tuner part provides via discrete LC low-pass filters an I and Q baseband output signal to a TDA8083 Satellite Demodulator and Decoder IC (SDD).
- ***Channel decoder part:***
  The I and Q baseband signal from the tuner part is fed to the TDA8083 channel decoder.
  The TDA8083 is intended for the reception of variable symbol rate DVB compliant MPEG2 signals (between 12 and 30 MS/s), transmitted via satellite. Also the TDA8044, which is pin and software compatible, can be used in this application which could allow a larger symbol rate range. In combination with the tuner part, all functions are available to deliver a corrected transport stream given an DVB encoded BPSK/QPSK signal.

The application note AN99003 of the OM5727 explains in more detail the use of the SDD and the measurement interface OM5711/M/C2.

1.1 Functionality of the Demo Board OM5729

The desired channel frequency is synthesizer controlled by a low phase noise synthesizer TSA5059, allowing to down-convert QPSK modulated satellite RF signals between 950 MHz and 2150 MHz with symbol rates between 12 and 30 MS/s, according several specifications that can be found in today's market (e.g.: CANAL+).

The demo board contains a LNA (RF pre-stage with a one wideband NPN transistor-stage amplifier delivering about 15 dB gain, and 4.5 dB Noise Figure) and an external AGC circuit by means of a single pin-diode, able to deliver about 15 dB of AGC. There is no band-pass filter 950 .. 2150 MHz and also no tracking filter implemented. The use of a tracking filter depends on the number of channels (and their power) reaching the RF input stage.

Automatic or manual AGC adjustment can be selected by means of a jumper "J1". In automatic AGC operation the TDA8083 SDD IC controls the AGC voltage. In manual AGC operation the AGC can be controlled with an external supply voltage of + 0.5 V up to +4.5 V applied to pin "P11" (V_{agc}).
WARNING:
To avoid damaging the IC TDA8060, the voltage on AGC control pin "P11" may not exceed +5V!

In paragraph 3.5 the AGC options of the OM5729 are explained.

1.2 The TDA8060

The direct conversion QPSK demodulator is the front-end receiver dedicated to digital TV broadcasting.
The wide range oscillator covers American, European and Asian satellite bands as well as the future SMA-TV US standard.
Accurate QPSK demodulation is ensured by the on-chip loop-controlled phase shifter. The zero-IF concept discards traditional IF filtering and intermediate conversion techniques. It also simplifies the signal path.

The baseband I and Q signal bandwidth only depends, to a certain extent, on the external filter used in the application.
Optimum signal level is guaranteed by a gain-controlled amplifier at the RF input. The GAIN pin (pin 4) sets the gain for both I and Q channels, providing a 30 dB range.
The chip also offers a selectable internal LO prescaler (divide-by-2) and buffer that has been designed to enable the use of terrestrial (cheaper) frequency synthesizers.

1.3 The TSA5059

The TSA5059 is an I^2C bus controlled single chip PLL frequency synthesizer designed for satellite and terrestrial tuning systems up to 2.7 GHz.
The RF preamplifier drives the 17 bit main divider enabling a step size equal to the comparison frequency, for an input frequency up to 2.7 GHz. The RF divider is working for frequencies up to 2.7 GHz, without the need for the divide by two prescaler to be used. A fixed divide by two additional prescaler can be inserted between the preamplifier and the main divider to give a software compatibility with existing IC's. In this case, the step size is twice the comparison frequency.
Both divided and comparison frequency are compared into the fast phase detector which drives the charge-pump. The loop amplifier is also on-chip, including the high-voltage transistor to drive directly the +30 Volts tuning voltage.

In the current version of the TSA5059, I^2C crosstalk level was found to be higher as expected. Although the IC is fully functional, to avoid the I^2C crosstalk problem, an external NMOS is added ("TR101" - BSN20) to replace the internal loop amplifier and high voltage transistor. The use of the NMOS is explained in paragraph 3.6.

1.3.1 I^2C address select

Control data is entered via the I^2C bus. The device has four programmable addresses, enabling the use of multiple synthesizers in the same system, programmed by applying a specific voltage to pin 4 "AS" of the TSA5059. On the OM5729, the required voltage can be applied by means of a resistive voltage divider "R50" and "R51", see Data Sheet of the TSA5059. In normal operation, if resistors "R50" and "R51" are not mounted (pin 4 of TSA5059 left open), the I^2C address C2 must be used. An easy way to test if the TSA5059 responds, is to enable output port "P3" in the *Tuner - TSA5059* menu of the DBUI software. The LED "D1" should light up.

1.4 OM5729 Specifications

+5 V supply voltage:	min.: +4.75 V, max.: +5.25 V
+28 V supply voltage:	min.: +28 V, max.: +33 V
Frequency range:	950 .. 2150 MHz
Tuning Increment:	125 kHz (optimized loop filter)
Input level:	- 65 .. - 25 dBm
Input impedance:	50 Ohm (i.s.o. 75 Ohm, for measurement purposes)
Input return loss:	min. 8 dB
Noise Figure:	typical 5 dB
Low pass filter bandwidth:	typical 25 MHz
Symbol rate:	12 to 30 MS/s (limited by SDD IC TDA8083)
Convolutional code rates:	1/2, 2/3, 3/4, 5/6, 7/8
Implementation loss:	max. 0.8 dB with BER after Viterbi 1E-4, according Canal+ spec.

2. GETTING STARTED

This chapter describes step by step the installation of the OM5729 system package.

2.1 The OM5729 System Package

The OM5729 system package contains the following:

Hardware:

- OM5729 demo board, pcb number PR39233
- OM5711/M/C2 measurement interface + flat cable to connect to demo board PR39233
- I^2C interface board + 4-wire cable to connect to demo board PR39233

Software:

- OM5729 DBUI MS Windows (3.x/95) software

Documentation:

- This application note AN99018
- OM5729 DBUI software manual
- Data Sheet TDA8060
- Data Sheet TSA5059
- Data Sheet TDA8083

2.2 The OM5729 Demo Board

The OM5729 is a DVB-S satellite Network Interface Module (NIM), where the LNB output signal is processed to a DVB compliant transport stream. The OM5729 demo board is shown in Figure 1.

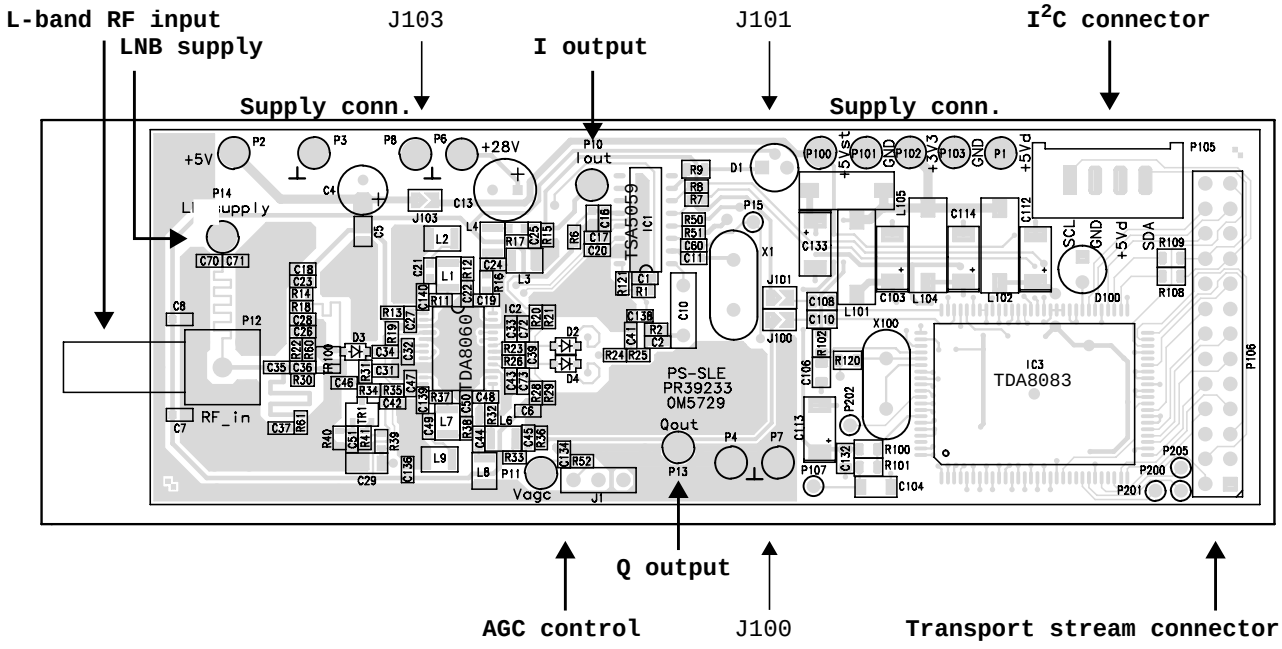

Fig.1 The OM5729 demo board

In Figure 2 the functional block diagram of the OM5729 application is shown

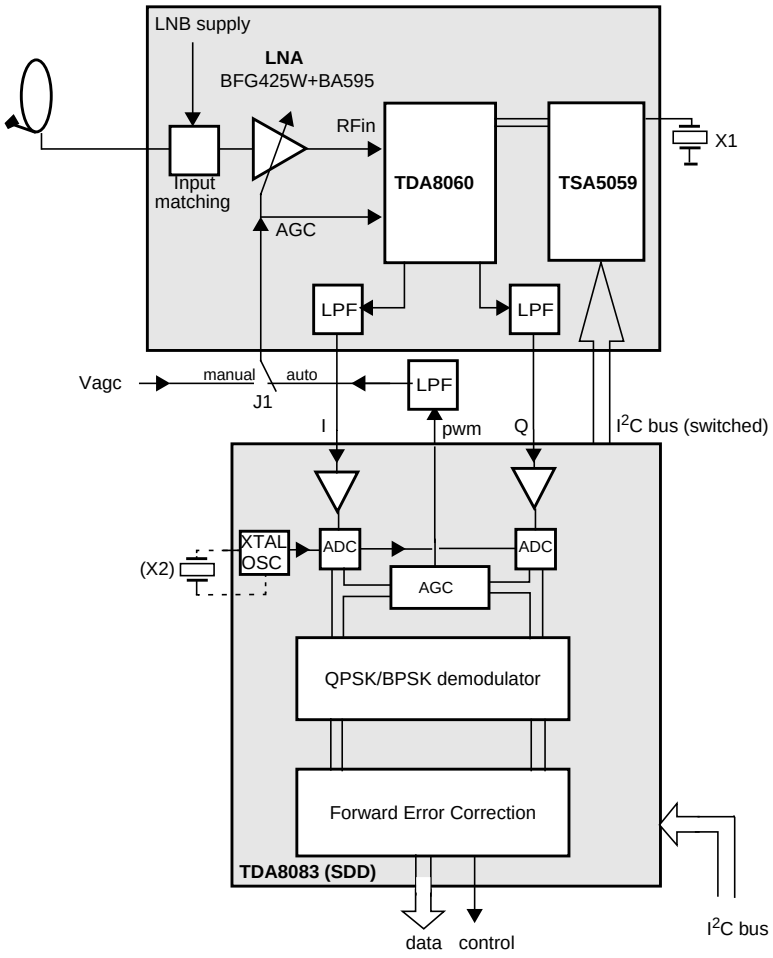

Fig.2 Functional block diagram of the OM5729 application

2.2.1 The solder jumpers at the top side of the board

On the top side the solder jumpers “J100” and “J101” connect the I and Q output from the tuner part to the SDD part.
At the top side solder jumper “J103” connects supply pin “P2” (+ 5V supply TDA8060) with supply pin “P100” (+ 5 V_{st} supply for interfacing the TDA8083 to the TDA8060). Default this solder jumper should be closed (soldered). In this case “P100” should be left open (no external supply voltage connected). If the TDA8060 is evaluated without TDA8083, this solder jumper should be opened.

2.2.2 TDA8083 versus TDA8044 application

At the bottom side, solder jumper “J104” is found (Clock Frequency Selection: CFS). See Figure 3. This solder jumper is added to provide compatibility with the TDA8044(H). In case a TDA8044H for 1 to 45 MS/s operation is mounted, this jumper should be left open. The internal clock is then set to 96 MHz. The system clock settings in the OM5729 software should be set according to the selection you make with this pad.

(Note: Only for test purposes; this demo board is not optimized for the use with symbol rates above 30 MS/s).

With the use of the TDA8044A, this jumper should be closed (soldered). The internal clock is then set to 64 MHz. Default, with the use of the TDA8083, this jumper should always be closed (soldered).

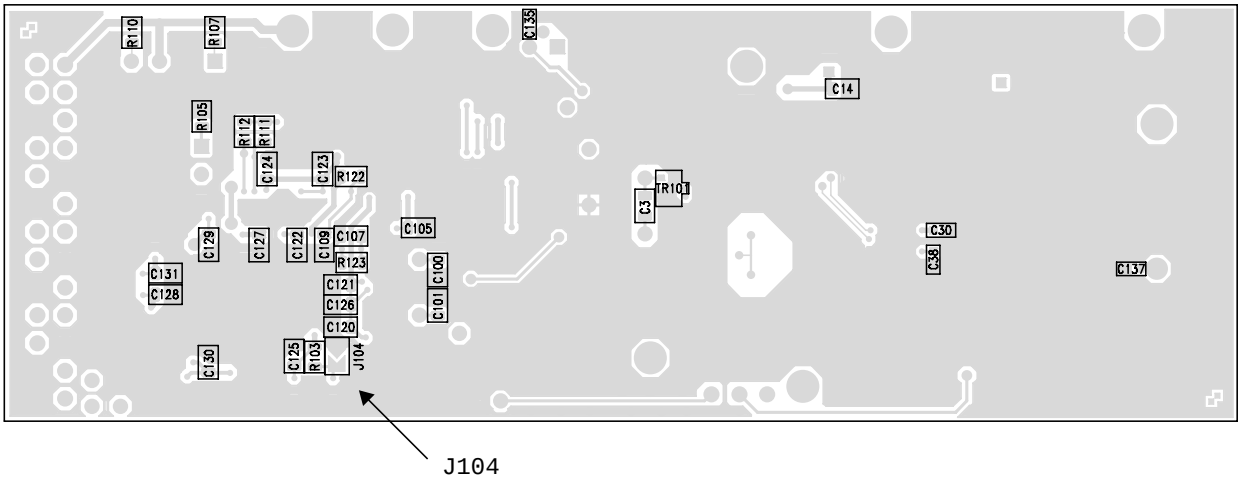

Fig.3 The bottom side of the PCB with solder jumper “J104”

2.2.3 Connectors of the OM5729 demo board

The supply voltage connectors:

P2: +5 V TDA8060 board supply input.
P3: Ground TDA8060 board supply.
P6: +28 V TDA8060 tuning supply voltage.
P8: Ground TDA8060 board supply.
P100: +5 V_{st} TDA8083 interfacing to TDA8060. Only needed if “J103” is open.
P101: Ground.
P102: +3.3 V SDD TDA8083 power supply.
P103: Ground.
P1: + 5 V_d I^2C bus supply voltage.
P11: External AGC voltage input: +0.5 V .. +4.5 V: +0.5 V = min. gain, +4.5 V = max. gain. (Only needed if “J1” is set to external AGC).
P14: LNB supply (e.g.: +14 / +18 V / 22 kHz).

Other connectors:

P105: I^2C 4-wire interface connector (SCL, GND, +5 V, SDA).
P106: Transport stream and measurement interface connector.
P12: RF input SMA connector (50 Ohm).
P10: $I_{baseband}$ output (note: Output can not be loaded with 50 Ohm).
P13: $Q_{baseband}$ output (note: Output can not be loaded with 50 Ohm).
P15: f_{xtal} or f_{comp} signal output (for measurement purposes; Only active if “C60” is mounted and TSA5059 is programmed accordingly).
P4: Extra ground for measurement purposes (e.g.: ground of probe).
P7: Extra ground for measurement purposes.
J1: AGC jumper to select between external or automatic AGC control.

2.3 The OM5711/M/C2 Board

The OM5711/M/C2 measurement interface board is shown in Figure 4. This board can be used to analyse the transport stream data of the SDD on the OM5729. This interface board provides connections to a BER receiver and a constellation analyser.

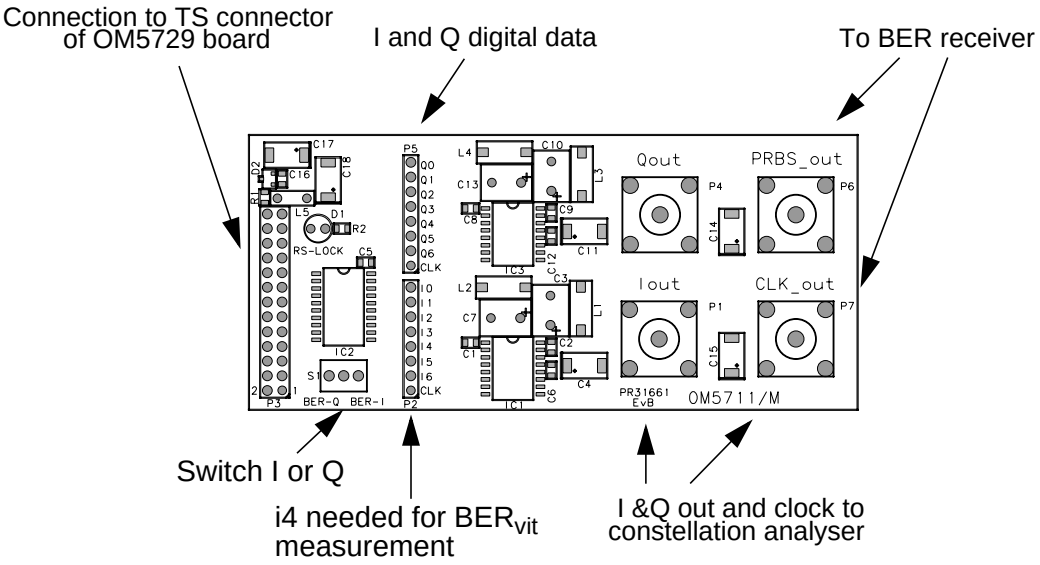

Fig.4 The OM5711/M/C2 measurement interface board

2.4 The I²C Interface Board

On the I²C interface board (PR30921or similar type) the jumpers can be removed to disable the on board pull-up resistors. These resistors are already present on the OM5729 board.

2.5 The OM5729 DBUI Software

The OM5729 DBUI software is a MS Windows (3.x/95) based control program, developed for user friendly I²C control. Installation and operation are explained in the OM5729 DBUI User Manual.

2.6 Installing the Board step by step

2.6.1 Power supply requirements

- P102: +3.3 Volt, 1Amp (260 mA nominal, depending on symbol rate).
- P100: +5 Volt_st. Not connected. Be sure that “J103” on the top side of the PCB is closed.
- P1: +5 Volt (digital), 0.1 Amp (depending on clock and symbol rate).
- P2: +5 Volt 0.5A (140 mA nominal).
- P6: +28 Volt, 5mA, PLL tuning voltage.

2.7 Connecting the OM5729 Board

- Connect I^2C connector to the I^2C interface board at the PC parallel port
- Connect OM5729 board with OM5711/M/C2 using the flat cable provided
- Connect a constellation analyser (if available) to connecters marked IOUT and QOUT on the OM5711/M/C2 board. The clock output and PRBS output are available on the same board.
- Apply a QPSK signal at first satellite IF frequency (950 .. 2150 MHz, from generator or LNB/dish) level between -65 and -25dBm.
- Connect the power supply pins according to paragraph 2.2.3.

2.8 Getting the Board in Lock

A detailed overview and explanation of all the software buttons and menus are discussed in the document called “OM5729 User manual DBUI software”. The only difference with the OM5719 software is the different SDD used: TDA8083 instead of the TDA8044.
NOTE: The DBUI software of the TDA8044 can also be used with OM5729, apart from some TDA8044 related settings which are not valid for the TDA8083 and vice versa.

- Start the DBUI software.
- Check in the “VERSION” menu if TDA8083 and the Tuner are present. If not present check if the connection from the computer to the application board is correct. If the TDA8083 is present, but the tuner is not, check if the “I^2C TUNER” setting in the “TUNER TSA5059” menu is enabled.
- Set in the “CHANNEL RELATED SETTINGS” menu the correct clock frequency (“system clock” = 64 MHz for normal use with OM5729 and the required Symbol rate.
- Select the frequency band and polarization for the desired channel in case a dish is used as input source by means of an external applied LNB supply voltage (14 V, 18 V, 22 kHz) on pin “P14”. The hardware to generate 22 kHz is not implemented on the OM5729.
- Enable in the “TUNER TSA5059” or “CHANNEL RELATED SETTINGS” menu the “I^2C TUNER” setting.
- Set in the “TUNER TSA5059” or “CHANNEL RELATED SETTINGS” menu the correct tuner frequency (950 MHz .. 2150 MHz).
- Monitor in the “TUNER” menu if the tuner is in lock.
- Set in the “TUNER” menu the correct Charge Pump Current according to the VCO frequency, the TSA5059 prescaler and the External prescaler to OFF, the Comp. Freq. to 125 kHz and the Intermediate Freq. to 0.00 MHz (Zero-IF). The Freq. Step (tuning grid) can be freely chosen by means of the up and down buttons.
- Monitor the Coarse AGC level; its value should be between 0 and 255. The highest level corresponds to the highest tuner gain. Set the correct Forward Error Correction parameters if needed.
- Monitor the FEC (Puncturing rate, no spectral inversion, Viterbi decoder locked, De-interleaver locked, complete FEC locked).
- For MPEG output choose: “Normal operation”. For constellation output or BER measurement via the measurement interface, choose: “demodulator evaluation”. Select the desired output format:
  A) normal operation, **B)** for constellation or **C)** BER measurement after Viterbi.

2.9 Trouble-shooting

In case the procedure discussed in paragraph 2.8 is used and the TDA8083 does not lock, check items below:

- Check the tuner AGC Voltage (test pin “P107”). It should be stable and between 0.5 and 4.5 Volt.
- Check the level of the I and Q signal on test pins “P10” and “P13” marked I_{out} and Q_{out}. The level should be 0.5 .. 0.8 V_{pp} for both. If not, check in the software if the setting mentioned above is set correctly. If necessary adjust the fixed gain setting until the level is correct. If no signal is found check with a spectrum analyser the signal delivered from LNB or generator. Make sure that the LNB gets the correct supply voltage (externally because the board cannot deliver this voltage) and the spectrum analyser is DC blocked. The marker of the spectrum analyser cannot directly be used to measure the signal level because the signal power is distributed over the signal bandwidth. So the actual level is higher (roughly 10*log (Bandwidth in dB)). If you use a generator the modulation can probably be switched off to measure the level.
- In case the FEC cannot lock, check also clock lock besides demodulator lock because demod lock can give a (false) lock on unmodulated carriers, analogue signals (such as sine waves), etc.
- The demodulator can false lock which can be recognized as having carrier and clock lock but no or no clear FEC lock. Making a frequency step with the tuner of $f_{symbol}/10$ up or down can solve this.
  The carrier loops have to be disabled before making the tuner step.
- Monitor Clock lock; For lock, clock lock level > Lock threshold level.
  For larger S/N ratios (> 6 dB) the clock lock level is higher than 1000 when in lock.
- Check if the carrier recovery parameters are correct.
- Monitor the demodulator lock; the demodulator lock threshold level is default set to 48.
  The AFC1 frequency read-out is only valid when clock and carrier loops are in lock.
- Monitor the BER, number of corrected and lost blocks to see the quality of the received channel.

3. OM5729 APPLICATION

This chapter provides more detailed application information on specific blocks of the OM5729.

3.1 The TDA8060 Block Diagram

The TDA8060 is a direct conversion (zero-if) QPSK down converter. The block diagram shows the functional internal blocks and the external blocks which are needed in the application. See Figure 5.

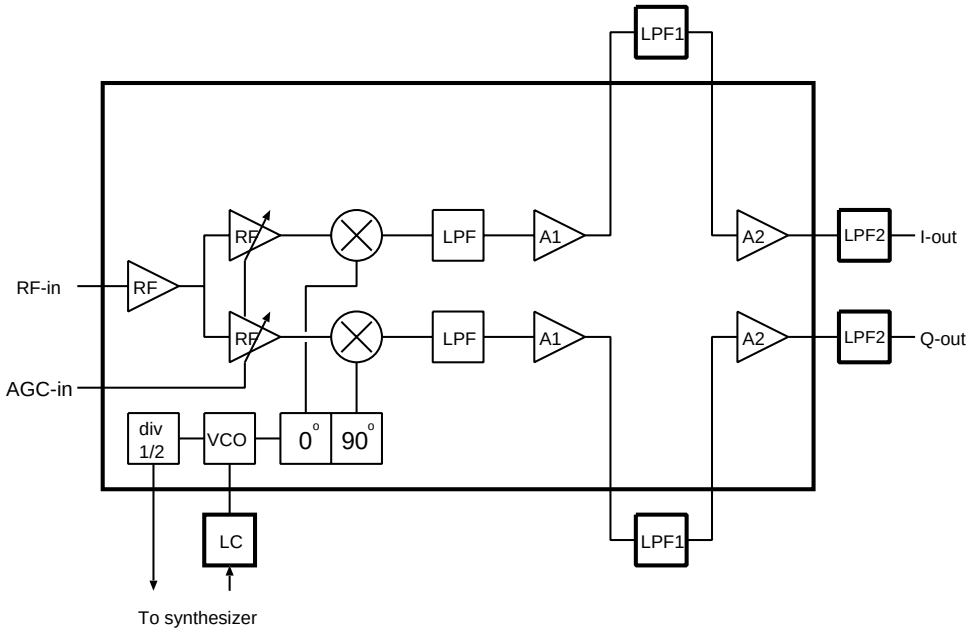

Fig.5 TDA8060 block diagram

The RF input signal is converted into two base band signal streams with a phase difference of 90 degrees. The VCO tuning range is equal to the receiver frequency range. The baseband signals are ‘near zero IF’, there is no carrier lock. Two internal low pass filters with -3 dB cut off frequencies of 100 MHz avoid overload of the first baseband amplifiers. The actual baseband filtering is done by the external low pass filters LPF1 and LPF2. The filtered baseband signals I and Q are connected to a TDA8083 for further signal processing.

3.2 The RF Input Matching and LNB Supply

The RF input stage is shown in Figure 6. The RF input connector “P12” has an input impedance of 50 Ohm. The input return loss is typical 10 dB. Complex impedances are created by using capacitors and / or microstrip lines. The LNB supply is part of the matching network.

In case a dish is used as input source, the polarization for the desired channel can be selected by means of an external applied LNB supply voltage (14 V, 18 V, 22 kHz) on pin “P14”. The hardware to generate 22 kHz is not implemented on the OM5729.

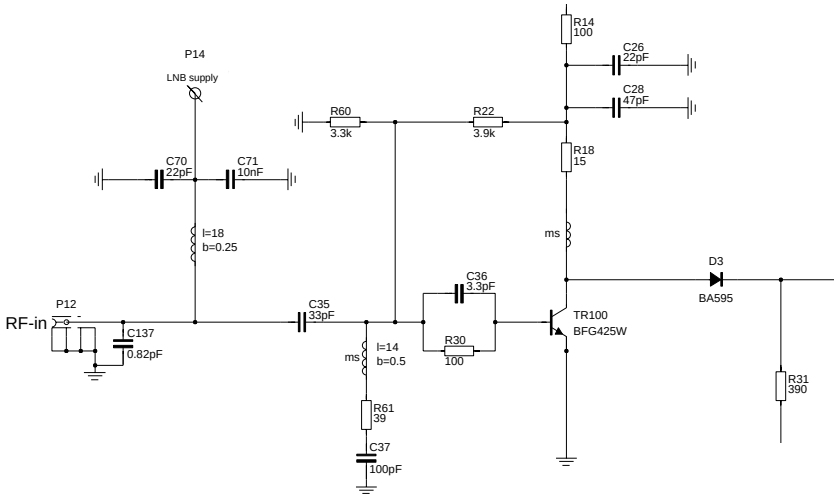

Fig.6 The RF input application

3.3 The VCO Circuit

The VCO coil inductance is critical. On the PCB the coil inductance is optimized for minimum size to enable maximum ground plane around it. This reduces unwanted coupling to and from other parts of the circuitry. The coil design has been changed since the first experimental design from a meander shape into a concentric shape. We do not claim to have found the optimal tank circuit, but this new design is more compact. The internal bonding wires and the internal (parasitic) capacitance of the TDA8060 in combination with the impedance seen between pin 17 and 18 (of the TDA8060) can create a parasitic tank circuit. To lower the Q factor of this parasitic circuit, relative to the Q factor of the wanted resonance, two resistors of 8.2 Ohm are placed. The varicap bias resistor values (“R21” and “R29”) are optimized for the lowest phase noise and have a value of 2.2 kOhm. See Figure 7.

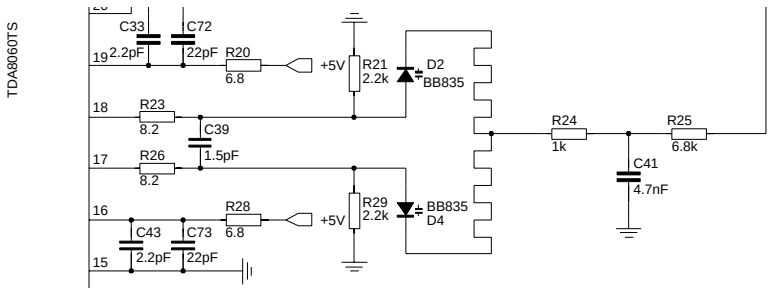

Fig.7 The schematic diagram of the VCO tank circuit

In Figure 8 and Figure 9 the layout of the VCO tank circuit is shown. Please note that the symmetrical tracks between the buffered LO outputs of the TDA8060 and the RF inputs of the synthesizer are placed closed to each other, narrow track width and as far away from the printed VCO coil as possible. This is done to minimize the radiation from these tracks.

The ground underneath the printed VCO coil is removed to reduce stray-capacitance from the coil to its surrounding. This is needed to capture the full tuning range. The via's in the VCO coil are part of the total inductance.

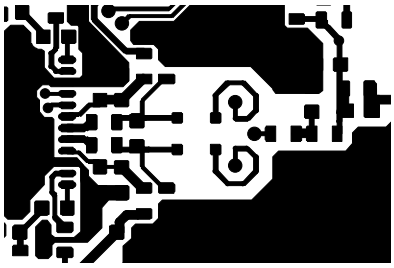

Fig.8 PCB copper at top layer

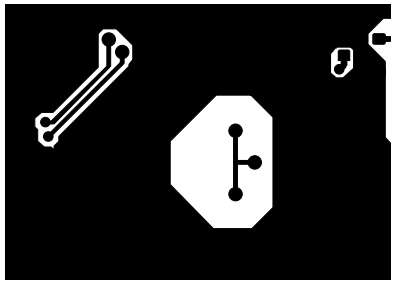

Fig.9 PCB copper at bottom layer, seen through the PCB

3.4 The Low Pass Filters

The low pass filters on demo board OM5729 are adapted to the specification of the TDA8083. The TDA8083 has Analogue to Digital Converters with a sample frequency of 64 MHz. The filters on the demo board are designed for a flat frequency response and time delay in the pass band 0 to 25 MHz and minimal 40 dB suppression above 45 MHz (maximum suppression at the sample frequency). This design is optimised to be used for symbol rates up to 27.5 MS/s.

The low pass filters can be further optimized.

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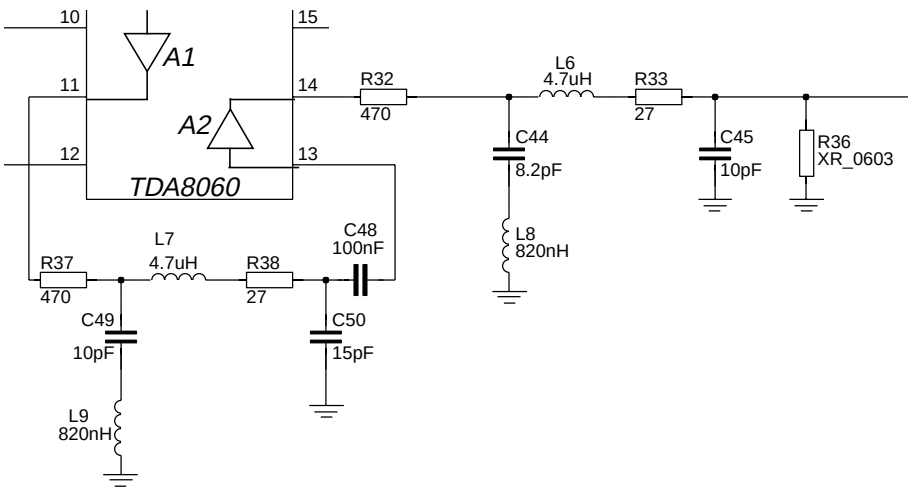


Fig.10 The low pass filters

Two filter sections are needed to get maximum adjacent channel rejection. See Figure 10. The first and second low pass filters have different trap capacitors (10 pF and 8.2 pF).
Although the output impedance of the amplifiers is about 50 ohms, the load impedance should be minimal 400 Ohms, because the amplifiers are not capable to deliver high currents.
If no filters are connected to the TDA8060 for test purposes, the amplifiers A2 will oscillate at about 15 MHz. This oscillation can be suppressed by adding a 1 nF capacitor from the amplifier inputs to ground.

The combined filters LPF1 and LPF2 give the following performance. See Figure 11 and Figure 12:

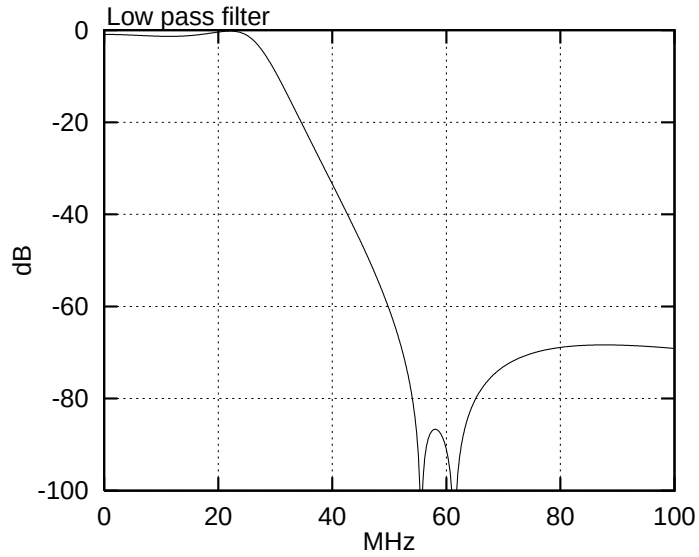


Fig.11 The low pass filter frequency response

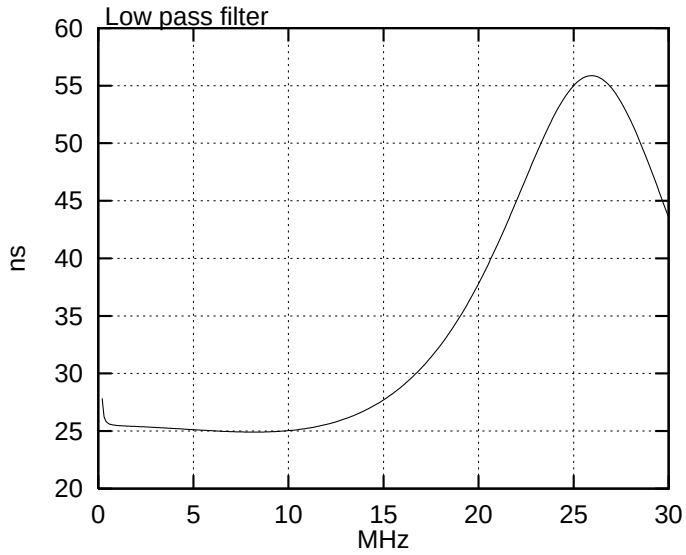


Fig.12 The low pass filter group delay

3.4.1 Low pass filter bandwidth and LNB drift

The low pass filters on the tuner part of the board have a bandwidth of about 25 MHz. This bandwidth fits the specification of the TDA8083. For 45 MS/s with the use of e.g. the TDA8044H, this filter is not wide enough to pass the signal without distortion. (With a roll-off factor of 0.35, you would expect a minimum bandwidth of 30 MHz. However, cutting the outer part of the spectrum does not give large degradations in BER. And in fact most satellites only transmit 1.2 times the symbol rate for a roll-off of 35%.

A common problem in satellite reception is drift of the incoming QPSK/BPSK signals since LNB oscillators are free-running ceramic resonator types, i.e. the receiving frequency is not stable. The reason for this is that the signal that is transmitted by the satellite in Ku- band (around 11GHz) is converted to a frequency in L-band (950MHz to 2150MHz) by means of an oscillator in the Low Noise Block converter (LNB) oscillating at 9.75GHz or 10.6GHz (these are common values). A transmitted 11GHz signal is at the satellite tuner input received as 11.00 - 9.75 = 1.250 GHz or 1250MHz. This LNB is mounted in the dish outdoors. Due to the large temperature changes outside, the frequency can drift plus or minus 5 MHz. The actual frequency drift depends on the specification of the LNB manufacturer. To cope with this drift two options are available:

1. Adjust the tuner synthesizer so that the IF signal remains near zero:
   Advantage:
   No risk for signal distortion, because the baseband spectrum does not drift outside the baseband filter.
   Disadvantage:
   A synthesizer step can cause lock-out.
2. Use a wider low pass filter than necessary for the symbol rate:
   Advantage:
   No risk of lock-out due to frequency steps.
   Disadvantage:
   More noise and adjacent channel power will get in to baseband.

With the 25 MHz low pass filter and taking into account option 2, the maximum symbol rate is about 30 MS/s. For symbol rates higher than 30 MS/s the low pass filter bandwidth must be adapted.

3.4.2 Definition of the I and Q baseband input signals.

The selective element in the receiver in front of the TDA8083 is the low pass filter. Since the symbol rate can change, and so will the bandwidth of the modulated signal, also adjacent/interfering channels can pass through the low pass filter. The low pass filter bandwidth used on the tuner part of the board is 25 MHz. A number of possible situations is shown in Figures 13 to 15:

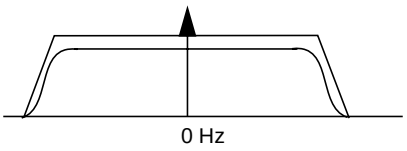


Fig.13 MCPC input signal

Multi channel per carrier (MCPC): In this case the QPSK/BPSK modulated signal fits within the passband of the low pass filter. All adjacent channels are suppressed sufficiently.

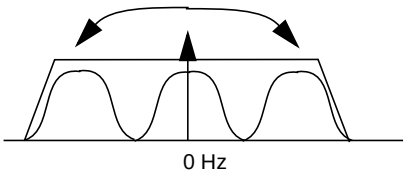


Fig.14 SCPC input signal

Single channel per carrier(SCPC): Together with the wanted modulated signal also some unwanted digital modulated signals are passing the low pass filter. These unwanted channels will result in baseband as adjacent channel interferences and need to be filtered out in the digital domain.

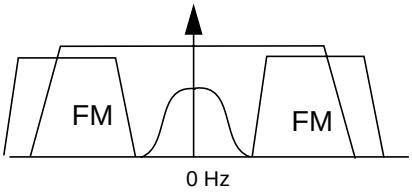


Fig.15 Simulcast input signal

Simul-cast situation: The QPSK/BPSK modulated signals have FM modulated signals as adjacent channels. The power of these FM modulated signals is generally higher than the digital modulated signal. Also in this situation, these FM modulated signals will cause adjacent channel interference.

3.4.3 The I and Q output pins

If the TDA8060 is evaluated without SDD, I and Q outputs are available at test pins “P10” and “P13”. These test pins must be loaded with high impedances, e.g. high-ohmic probes with input capacitance less than 1 pF.
If jumpers “J100” and “J101” are open, the input impedance of the TDA8083 must be imitated with 10 kOhm resistors “R15” and “R36” (normally not mounted) and the values of capacitors “C25” and “C45” can be adapted to compensate the probe capacitance. Otherwise the filters are not matched. See also Figure 10.

3.5 The AGC

Two situations are shown in Figure 16.

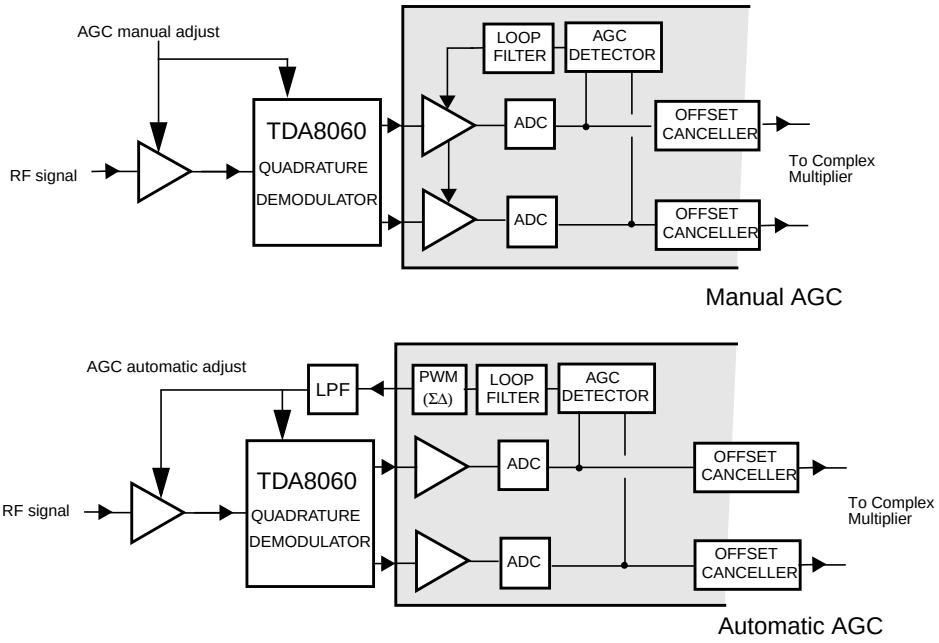


Fig.16 Possible configurations for the AGC

3.5.1 Automatic AGC

In this case the TDA8083 provides the tuner part of the board with an AGC feedback signal.

The pulse width modulator (PWM) converts the 8-bit loop filter output value to a bit stream on the output pin, V_{agc}. This output pin has an open drain configuration. This makes it possible to pull it up to 5 V output level. This is done by connection pin 94 via a resistor of 470 Ohms (“R100”) to +5 V_{st}, giving a maximum current of 10.6 mA. The maximum current that can be delivered by the output pin is 12 mA. This should preferably be a stable +5 V supply (+ 5 V_{st}, via “P100” or “P2”) because any ripple on this supply will also be present on the AGC voltage on the tuner.

An external low pass filter is required to convert the PWM-stream to a control voltage and to remove the high frequency noise signals. This can be done by a passive RC low-pass filter. A resistor (“R101”) of 4.7 kOhm in series from pin 94 (TDA8083) to V_{agc} of the tuner and a capacitor (“C104”) from V_{agc} pin of the tuner to ground of 150 nF are required, see Figure 17.

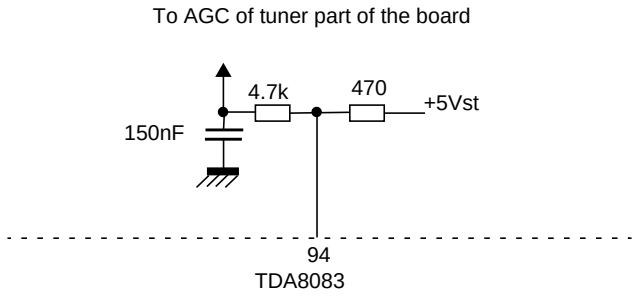


Fig.17 The application of the AGC filter

The AGC voltage varies from +4.5 V down to +0.5 V for tuner input levels from about -69 dBm to -10 dBm depending on the RF frequency.

3.5.2 Manual AGC

A manual AGC adjustment is implemented by means of an ‘external’ AGC control pin “P11” (V_{agc}). The AGC can be controlled by means of an external supply voltage of +0.5 V .. +4.5 V.
An AGC voltage of *+0.5 V = minimal gain.*
An AGC voltage of +4.5 V = maximum gain.

WARNING:
To avoid damaging the IC TDA8060, the voltage on AGC control pin “P11” may not exceed +5V !
A 1 kOhm resistor is added in series with “P11” to avoid damaging the IC.

The input impedance of “P11” is typical 30 kOhm.
For optimal noise figure performance, the demo board is designed in a way that the first 10 dB of attenuation are controlled by the TDA8060 mainly, from this point on the pin diode starts to attenuate as well.

For easy use, a (multi-turn) potentiometer of 5 kOhm can be connected to pin “P11” in order to control the AGC voltage without the need for an external supply voltage. See Figure 18.

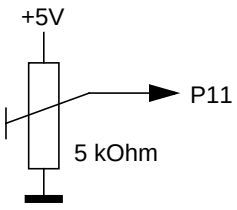


Fig.18 AGC control with potentiometer

3.6 The TSA5059 with External NMOS

The TSA5059 includes a loop amplifier and a high-voltage transistor to drive directly the +30 Volts tuning voltage between pin 1 (CP) and pin 16 (VT). While the internal high voltage transistor and the loop amplifier share the same ground pin as the I^2C bus, I^2C crosstalk problems can occur.

The easiest way to avoid any I^2C crosstalk is to make use of the I^2C switch which is implemented in the TDA8083. This allows to enable by software the I^2C bus traffic to the tuner part only when necessary.
If the tuner part is not addressed, the I^2C switch can be disabled by software.

If I^2C crosstalk is still a problem, the internal loop amplifier and high voltage transistor can be bypassed.
An external “high voltage” NMOS SOT23 SMD transistor BSN20 (“TR101”) is used. In this case, the external (high voltage) loop amplifier does not share the same ground with the I^2C bus any more.
The standard OM5729 application makes use of this external NMOS. In this case, the VT pin (16) is left open.

The OM5729 can also be evaluated without the external NMOS. In this case, the jumper resistor of 0 Ohm (“R121”) should be mounted, the BSN20 (“TR101”) should be removed.

The V_{ds_sat} of this NMOS transistor is below 20 mV. It’s also possible to use an equivalent (SMD) type NMOS, provided its threshold voltage is guaranteed < 2 V (charge pump DC range = 3 V).
The gate of the external transistor is placed as close as possible to pin 1 (high impedance CP pin) of the TSA5059. The source is connected to ground. An extra capacitor is added between the drain of the BSN20 and ground to prevent instable loop operation. This capacitor is placed close to the drain of the NMOS transistor. The value of this capacitor is small, so the loop filter parameters are not affected and the capacitor does not degrade the I^2C crosstalk performance itself. In our application 15 pF is used.

Measurement results have shown that with the external NMOS transistor the I^2C crosstalk is greatly reduced compared to the normal application without external transistor.

The reason for the use of an NMOS instead of e.g. a darlington transistor is because we fear some problems with the external darlington transistor application regarding tuning voltage range. A darlington transistor limits the tuning voltage at the low end to $1 \times V_{be} + 1 \times V_{ce\_sat}$.

3.7 TSA5059 Loop Filter Parameters

The loop filter of the OM5729 is designed for a step size (tuning grid) of 125 kHz, commonly used in satellite tuner applications. With the TSA5059, no divide by two prescaler is needed to cover the complete satellite tuning range. Therefore, the comparison frequency (f_{comp}) equals the step size: f_{comp} = 125 kHz. The TSA5059 enables the use of four different charge pump currents with a ratio of 10: I_{cp} = 120 uA, 260 uA, 555 uA and 1200 uA. These different charge pump currents can be used with the OM5729 application to optimize the loop gain of the synthesized loop by compensating the variable K_{vco}. This charge pump current must be set correctly in software depending on the RF frequency. Select:

- I_{cp} = 555 uA for VCO frequencies below 1100 MHz.
- I_{cp} = 260 uA for VCO frequencies between 1100 MHz and 1200 MHz.
- I_{cp} = 120 uA for VCO frequencies between 1200 MHz and 1600 MHz.
- I_{cp} = 260 uA for VCO frequencies between 1600 MHz and 1800 MHz.
- I_{cp} = 555 uA for VCO frequencies between 1800 MHz and 2000 MHz.
- I_{cp} = 1200 uA for VCO frequencies above 2000 MHz.

The loop filter components are chosen to achieve the optimal phase noise requirement result.
The loop filter parameters are simulated / calculated with the SIMPATA software tool of Philips.

3.8 Application for One Crystal Operation

The OM5729 application makes use of two crystals of 4 MHz (“X1” and “X100”). In this way, the tuner part and the SDD part can operate independently if one of the two parts is evaluated separately.
Normally, “X1” and “X100” are mounted, “C60” and “R120” are not mounted. In this case, the tuner TSA5059 software setting XT/COMP output should be set to *NONE*.
With the correct hardware and software settings, it’s also possible to use only one crystal (“X1”) in the total OM5729 application. The TSA5059 is chosen to operate with the one crystal because the TSA5059 contains a buffered f_{xtal} output (pin 3) which can drive the SDD. More important, the phase noise performance of the total system depends mainly on the crystal oscillator of TSA5059. therefore, it’s recommended to put the crystal at the TSA5059.
At power-on, the XT/COMP output (pin 3) of the TSA5059 is always enabled, with the crystal frequency signal of 4 MHz (f_{xtal}) selected. This signal can be used to provide the TDA8083 with the required clock signal.
In this case, The jumper resistor of 0 Ohm (“R120”) and “C60” (In the range of 1 nF to 10 nF (not critical)) should be mounted. “X100”, “C100” and “C101” should be removed. Please take care that all I^2C traffic to the TSA5059 sets the XT/COMP output to f_{xtal}. Otherwise, the TDA8083 will stop operation.

3.9 The I^2C Connector

The I^2C connector provides +5 V_d from the OM5729 board to the I^2C interface board via supply pin “P1”.
The demo board contains pull-up resistors (“R107” & “R110”) to the +5 V_d board supply. The resistor values are 10 kOhm. The I^2C bus traffic to the TSA5059 is fed through the TDA8083 by tri-state switches. This makes it possible to switch-off any I^2C traffic to the TSA5059 after tuning the synthesizer frequency.
Normally, Address Select (AS) pin 4 of the TSA5059 is left open and the I^2C address C2 must be used. Other I^2C addresses can be selected by adding a resistive divider by means of “R50” and “R51”. See also the Data Sheet of the TSA5059. An easy way to test if the TSA5059 responds, is to enable output port “P3” in the software. The LED D1 should light up.

4. MEASUREMENTS

This chapter describes the measurements performed on the OM5729 demo board, pcb nr. PR39233.
Most measurements described in this chapter are performed on the tuner part of the OM5729.
For these kind of measurements, the demo board should be set up accordingly, e.g. see chapter 3.

4.1 Charge Pump Current Setting

For optimal synthesizer loop filter performance the charge pump current (I_{cp}) must be set correctly in software depending on the RF frequency. Select, unless specified differently:

- **I_{cp} = 555 uA for VCO frequencies below 1100 MHz.**
- **I_{cp} = 260 uA for VCO frequencies between 1100 MHz and 1200 MHz.**
- **I_{cp} = 120 uA for VCO frequencies between 1200 MHz and 1600 MHz.**
- **I_{cp} = 260 uA for VCO frequencies between 1600 MHz and 1800 MHz.**
- **I_{cp} = 555 uA for VCO frequencies between 1800 MHz and 2000 MHz.**
- **I_{cp} = 1200 uA for VCO frequencies above 2000 MHz.**

4.2 RF Input Level vs. AGC Voltage

The AGC voltage is given in Figure 19 for 500 mV_{pp} output level for different RF input levels and three different RF frequencies. Charge pump current settings according paragraph 4.1.

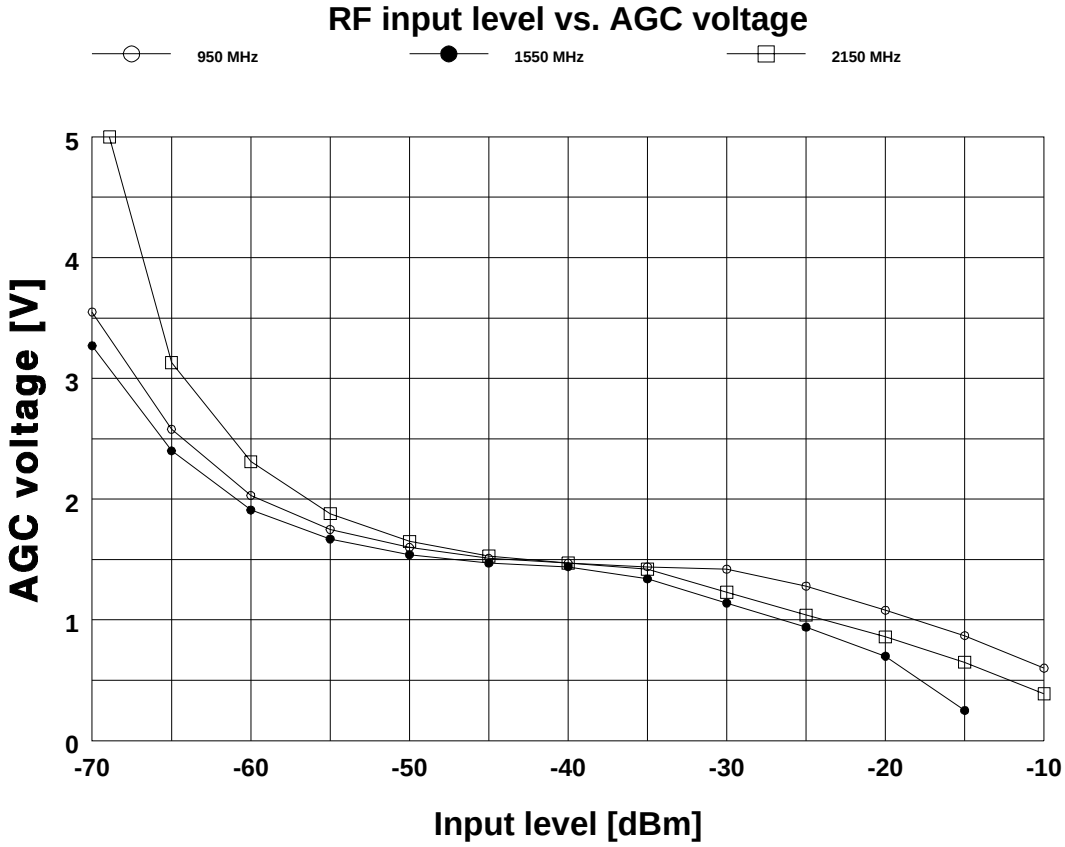


Fig.19 Typical external AGC voltage curve for 500 mV_{pp} I/Q out.

f_{vco} [MHz]	Input Level [dBm]													
	(+5V)	**-70**	**-65**	**-60**	**-55**	**-50**	**-45**	**-40**	**-35**	**-30**	**-25**	**-20**	**-15**	**-10**
950	-71.8	3.55	2.58	2.03	1.75	1.60	1.51	1.47	1.44	1.42	1.28	1.08	0.87	0.60
1550	-72.8	3.27	2.40	1.91	1.67	1.54	1.47	1.44	1.34	1.14	0.94	0.70	0.25	-
2150	-68.9	-	3.13	2.31	1.88	1.65	1.53	1.47	1.42	1.23	1.04	0.86	0.65	0.39

Table 1: RF input level vs. AGC voltage

4.3 Phase Noise Measurement

Measuring conditions with demo board OM5729:

- Phase Noise measured at I / Q baseband outputs at $f_{baseband}$ = 1 MHz for each charge pump current.
- Signal generator frequency $f_{rf} = f_{vco}$ + 1 MHz, level is - 25 dBm. The phase noise performance of used signal generator has to be significantly better than measured phase noise.
- V_{agc} is manually adjusted to 500 mV_{pp} I/Q baseband output signal voltage.

f_{vco} [MHz]	I_{cp} = 120 uA			I_{cp} = 260 uA		
	Phase Noise [dBc/Hz @1kHz]	**Phase Noise [dBc/Hz @10kHz]**	**Phase Noise [dBc/Hz @100kHz]**	**Phase Noise [dBc/Hz @1kHz]**	**Phase Noise [dBc/Hz @10kHz]**	**Phase Noise [dBc/Hz @100kHz]**
950	-56.8	-81.8	-99.8	-62.0	-81.1	-99.8
1050	-56.3	-81.1	-98.4	-62.5	-80.6	-98.4
1150	-55.7	-79.1	-98.1	**-62.8**	**-78.6**	**-98.1**
1250	**-55.0**	**-76.5**	**-98.6**	-62.5	-75.6	-98.3
1350	**-54.6**	**-76.1**	**-97.6**	-59.8	-75.1	-98.1
1450	**-55.0**	**-77.0**	**-97.8**	-59.5	-76.4	-98.1
1500	**-54.5**	**-78.1**	**-98.1**	-59.2	-77.1	-98.1
1550	**-54.0**	**-79.1**	**-99.9**	-59.3	-78.6	-98.9
1650	-53.0	-79.9	-99.5	**-58.6**	**-80.0**	**-99.4**
1750	-53.8	-81.1	-99.9	**-55.2**	**-80.8**	**-99.7**
1850	-52.0	-80.9	-99.6	-53.5	-81.4	-99.4
1950	-49.7	-81.1	-99.6	-54.0	-81.4	-99.9
2050	-48.5	-80.6	-100.1	-51.8	-80.3	-100.0
2150	-50.0	-79.6	-100.1	-52.3	-80.1	-100.0

Table 2: Phase Noise measurement with I_{cp} = 120 uA and 260 uA

f_{vco} [MHz]	I_{cp} = 555 uA			I_{cp} = 1200 uA		
	Phase Noise [dBc/Hz @1kHz]	**Phase Noise [dBc/Hz @10kHz]**	**Phase Noise [dBc/Hz @100kHz]**	**Phase Noise [dBc/Hz @1kHz]**	**Phase Noise [dBc/Hz @10kHz]**	**Phase Noise [dBc/Hz @100kHz]**
950	**-67.0**	**-80.5**	**-99.4**	-73.2	-78.5	-99.1
1050	**-68.3**	**-79.3**	**-98.6**	-73.7	-77.4	98.6
1150	-69.0	-76.6	-98.4	-	-	-
1250	-68.7	-73.6	-97.4	-	-	-
1350	-66.3	-72.3	-97.6	-	-	-
1450	-66.1	-74.1	-98.1	-	-	-
1500	-66.3	-75.8	-98.0	-	-	-
1550	-67.3	-76.6	-99.1	-	-	-
1650	-65.3	-78.6	-99.4	-68.8	-76.9	-99.4
1750	-61.5	-80.1	-99.6	-67.1	-78.8	-99.9
1850	**-59.7**	**-80.9**	**-99.4**	-66.0	-79.8	-99.2
1950	**-56.4**	**-81.3**	**-99.9**	-62.8	-80.1	-99.8
2050	-54.0	-80.9	-100.1	**-58.2**	**-80.4**	**-100.1**
2150	-52.0	-80.3	-99.5	**-54.5**	**-80.3**	**-99.8**

Table 3: Phase Noise measurement with I_{cp} = 555 uA and 1200 uA

The reference frequency breakthrough was found to be better than -67 dBc for all measurements.

More measurements on phase noise were performed to verify the optimal charge pump current setting vs. VCO frequency. The optimum phase noise curves are chosen from the tables (bold values) and shown in Figure 20:

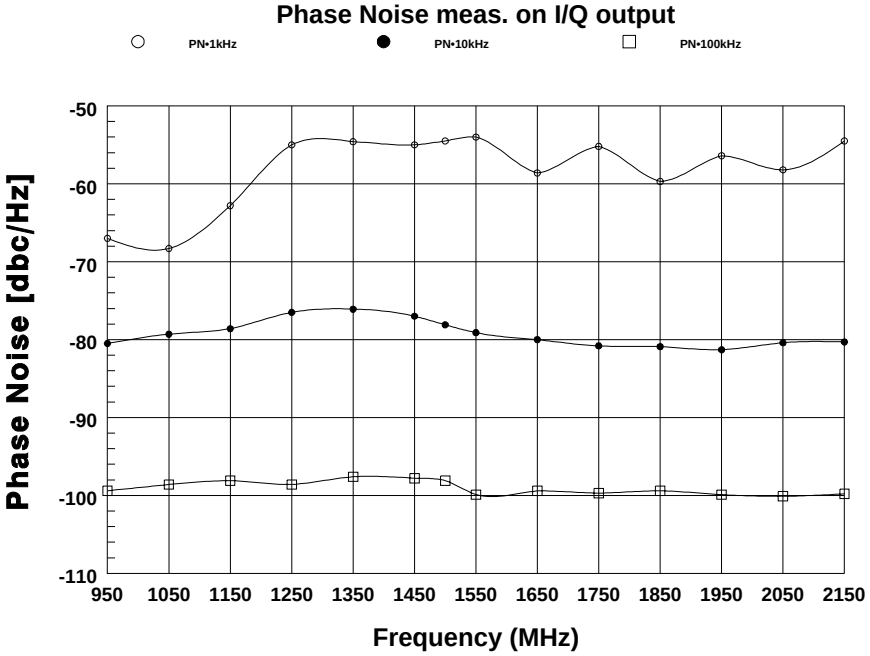


Fig.20 The phase noise performance of the synthesized VCO

4.4 Tuning Voltage and K_{vco} Measurement

The typical VCO tuning voltage and steepness K_{vco} is given below:

Frequency [MHz]	V_{tune} [V]	K_{vco} [MHz/V]
(921)	(56.3m)	-
950	0.60	48
1050	2.60	60
1150	3.85	100
1250	4.62	167
1300	4.92	182
1350	5.21	200
1450	5.82	143
1500	6.18	133
1550	6.59	111
1650	7.63	83
1750	9.04	59
1850	10.98	45
1950	13.66	32
2050	17.34	24
2150	22.35	17
(2229)	(28.00)	-

Table 4: VCO tuning curve and steepness

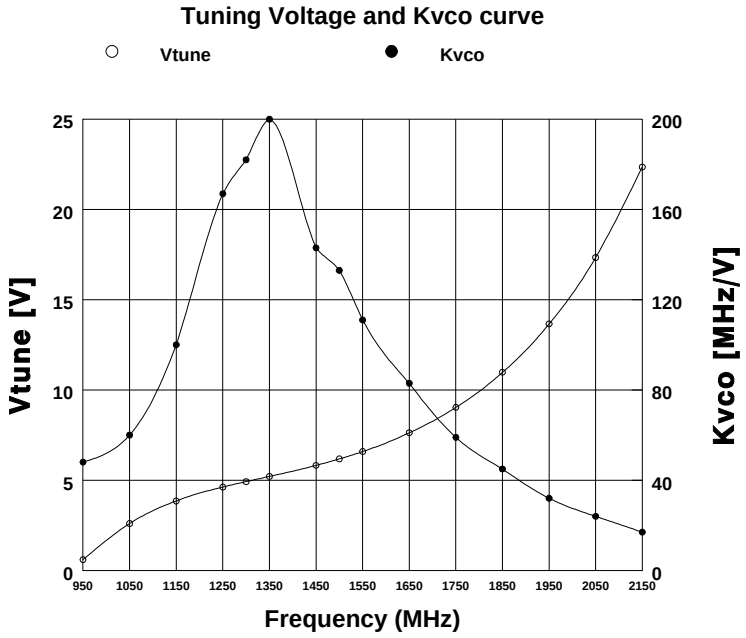


Fig.21 VCO tuning curve and steepness

4.5 LO Leakage Measured at the RF-Input

The measured LO power at the RF input gives an indication of the amount of isolation from the LO tank circuit to the RF input. Insufficient isolation between the LO tank circuit to the RF input might lead to degraded pulling behaviour.

4.5.1 Measurement setup

The measurement setup is shown in Figure 22.

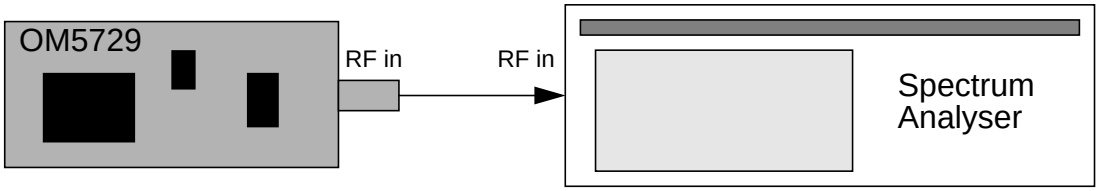


Fig.22 “LO leakage” measurement setup

4.5.2 Measurement procedure

- Connect the power supplies of OM5729.
- Adjust the AGC voltage at “P11” to +5 V or +0.8 V.
- Connect a spectrum analyser to the RF INPUT connector.
- Load the DBUI software.
- Select the correct (tuner) settings. Afterwards remove the I^2C connector.
- Set the frequency of the spectrum analyser to the same frequency as the VCO.
- Measure the absolute leakage power level.

f_{vco} [MHz]	**950**	**1150**	**1350**	**1550**	**1750**	**1950**	**2150**
P_o [dBm] V_{agc}=+5V	-98.0	-100.0	-98.0	-99.0	-87.2	-87.3	-82.0
P_o [dBm] V_{agc}=+0.8V	-93.8	-102.0	-93.0	-95.0	-92.5	-92.2	-84.8

Table 5: LO leakage level at the RF input connector

4.6 IM2 and IM3 Measurements

4.6.1 Measurement setup

The measurement setup is shown in Figure 23:

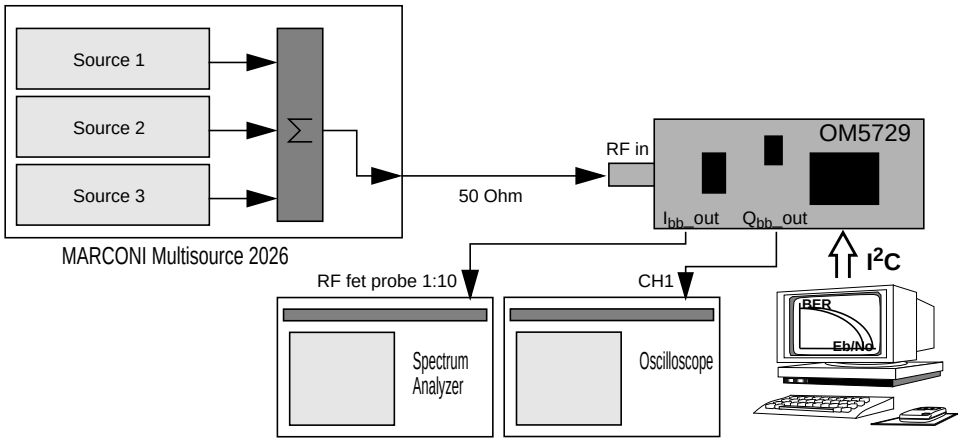


Fig.23 measurement setup IM2/IM3

4.6.2 Measurement procedure

- Setup measurement according to Figure 23
- Set the f_{vco} to 1498 MHz in the software
- Apply f_1 (f = 1500 MHz, e.g. P = -22 dBm) to the OM5729
- Adjust the AGC voltage to obtain an $I,Q_{baseband}$ output signal level of 500 mV_{pp}
- Apply f_2 (f = 1503 MHz, same power as f_1)
- On RF, the spectrum looks like Figure 24.
- In baseband, the spectrum is shown in Figure 25.
- Measure the distance of f(2MHz / 3MHz) for IM2.
- Measure the distance of f(2MHz / 1MHz) for IM3.

The IP figures (in dBm) can be derived from the IM figures (in dBc) according following formulas:

- IP2 = $|IM2| + P_{in}$ [dBm]
- IP3 = $|0.5*IM3| + P_{in}$ [dBm]

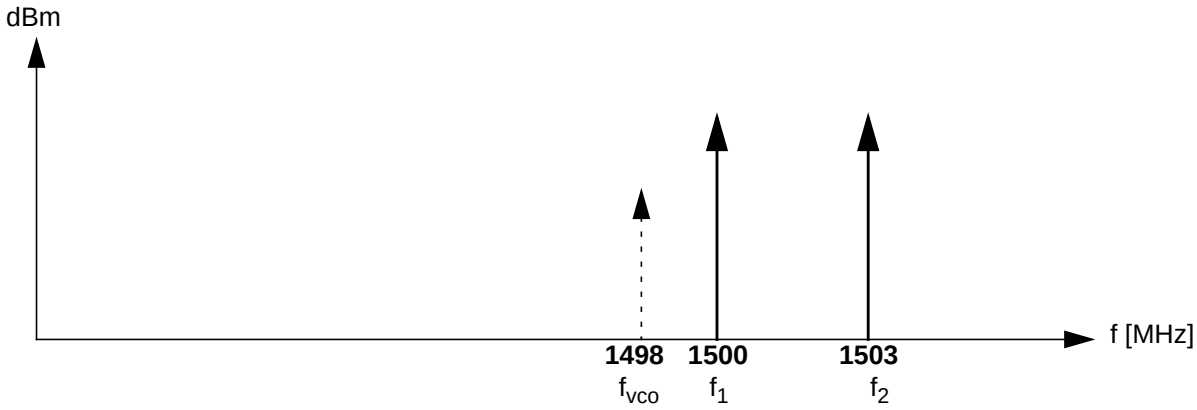


Fig.24 RF spectrum

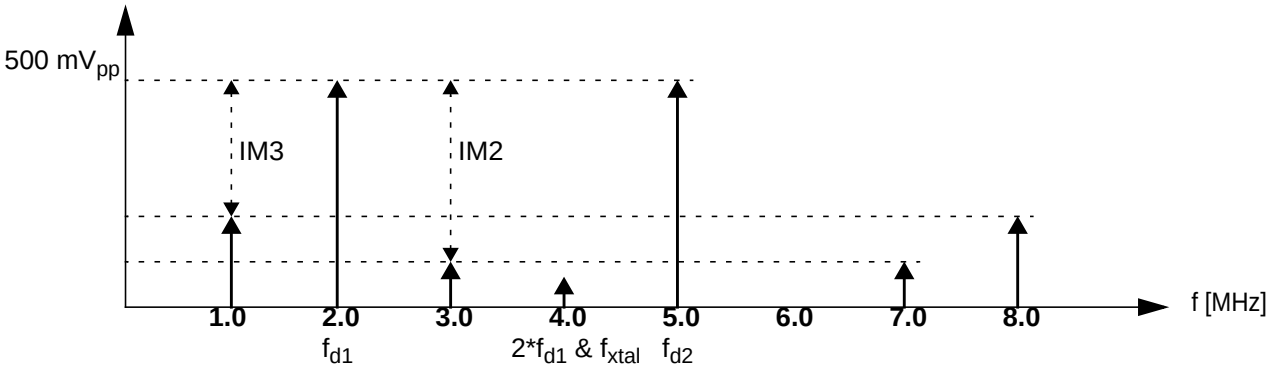


Fig.25 Baseband spectrum

4.6.3 Measurement results

In Table 6 input IM2 and input IM3 figures are shown.

f_{vco} [MHz]	f_1 [MHz]	f_2 [MHz]	f_{d1} [MHz]	f_{d2} [MHz]	P_{in2} [dBm] P_{in3} [dBm]	IM2 [dBc]	IP2 [dBm]	IM3 [dBc]	IP3 [dBm]
948	950	953	2	5	-22 -30	-46 -47	+24 +17	-41.8 -51	-1.1 -4.5
1498	1500	1503	2	5	-22 -30	-44.0 -45.4	+22 +15.4	-41.2 -44.5	-1.4 -7.8
2148	2150	2153	2	5	-22 -30	-40.3 -44.0	+18.3 +14	-46.3 -50.2	+1.2 -4.9

Table 6: Input IP2 and IP3 in-band measurement

4.7 I and Q Imbalance Measurement

Measurement setup:

- Set the desired f_{vco} frequency, e.g.: f_{vco} = 1500 MHz.
- Apply at the RF input of OM5729 a sine wave from a signal generator tuned to $f_{vco} + f_{offset}$, e.g.: 1500 MHz + 100 kHz = 1500.1 MHz.
- Adjust the level of the signal generator to the desired level and adjust the AGC for I and Q baseband output signals of 500mV_{pp}.
- The I and Q output pins are connected with high impedance probes to a vector voltmeter (HP85081B and HP8508A) which should be calibrated first.
- Before measuring, disconnect the I^2C connector.
  Measurement accuracy: 100 kHz offset: +/- 1dB, 1 MHz offset: +/- 0.2 dB.

f_{vco} [MHz]	Input power level [dBm]					
	-65		-45		-20	
	G [dB]	P [deg]	G [dB]	P [deg]	G [dB]	P [deg]
950	0.05	-89.5	0.05	-89.7	0.08	-89.5
1050	0.06	-89.7	0.03	-89.7	0.09	-89.5
1150	0.07	-89.5	0.05	-89.6	0.13	-89.5
1250	0.12	-89.3	0.18	-89.5	0.16	-89.5
1350	0.14	-89.2	0.10	-89.5	0.10	-89.2
1450	0.16	-89.0	0.12	-89.4	0.20	-88.3
1550	0.20	-88.9	0.18	-89.4	0.27	-88.9
1650	0.23	-89.5	0.18	-88.9	0.30	-88.2
1750	0.25	-89.4	0.26	-89.8	0.24	-89.3
1850	0.23	-89.2	0.28	-89.8	0.38	-88.1
1950	0.25	-89.4	0.32	-89.6	0.39	-87.8
2050	0.25	-89.4	0.32	-89.4	0.38	-87.5
2150	0.25	-89.2	0.32	-89.3	0.39	-87.6

Table 7: I/Q gain and phase imbalance measurement at 100 kHz offset

f_{vco} [MHz]	Input power level [dBm]					
	-65		-45		-20	
	G [dB]	P [deg]	G [dB]	P [deg]	G [dB]	P [deg]
950	0.08	-90.0	0.06	-89.7	0.05	-89.7
1050	-0.05	-86.9	-0.08	-89.5	-0.05	-89.2
1150	0.03	-89.2	0.02	-89.5	0.09	-89.4
1250	0.05	-89.3	0.04	-89.5	0.11	-89.3
1350	0.09	-89.2	0.06	-89.5	0.13	-89.0
1450	0.14	-89.1	0.10	-89.4	0.20	-88.6
1550	0.16	-88.9	0.16	-89.4	0.24	-88.4
1650	0.20	-88.9	0.20	-89.4	0.32	-87.6
1750	0.25	-88.9	0.29	-89.3	0.38	-87.7
1850	0.23	-88.8	0.29	-89.2	0.37	-87.3
1950	0.24	-88.8	0.31	-89.1	0.37	-87.1
2050	0.23	-88.7	0.37	-87.0	0.37	-86.9
2150	0.24	-88.6	0.31	-88.6	0.36	-86.9

Table 8: I/Q gain and phase imbalance measurement at 1 MHz offset

4.8 Temperature Sensitivity

The VCO tuning range, with the PLL in lock, and the RF sensitivity are measured at different temperatures. The measurement conditions are:

- I/Q baseband output 500 mV_{pp} constant
- V_{agc} = +5 V constant

Temperature [˚C]	RF sensitivity [dBm] f_{vco} = 950 MHz	RF sensitivity [dBm] f_{vco} = 1500 MHz	RF sensitivity [dBm] f_{vco} = 2150 MHz	Tuning lock range [MHz]
T = +85˚C	-70.3	-70.5	-66.4	916 .. 2212
T = +25˚C	-71.6	-72.9	-68.6	921 .. 2229
T = - 20˚C	-73.3	-74.5	-70.8	924 .. 2240

Table 9: Temperature effects on PLL lock range and RF sensitivity

4.9 Noise Figure and Voltage Gain Measurement

4.9.1 Measurement setup

The measurement setup is shown in Figure 26.

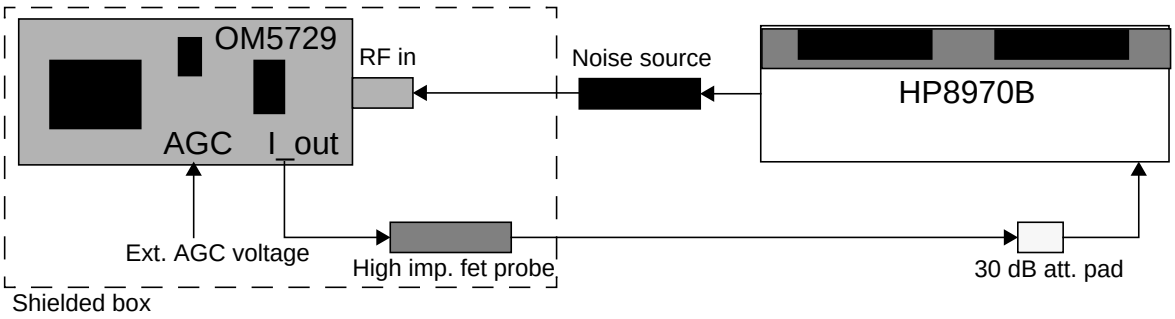


Fig.26 Noise figure and voltage gain measurement setup

The load impedance of the I/Q baseband low pass filters is about 10 kohm. Therefore the voltage gain is measured with respect to this load impedance.
The Noise Figure of the demo board is mainly defined by the LNA (and attenuation) in front of the TDA8060.

4.9.2 Measurement procedure

- Measured with HP8970B Noise Figure / Gain Analyser.
- V_{agc} = +5 V constant.

This measurement is intended for comparative use only.

f_{vco} [MHz]	**950**	**1050**	**1150**	**1250**	**1350**	**1450**	**1550**	**1650**	**1750**	**1850**	**1950**	**2050**	**2150**
Voltage Gain [dB]	69.2	70.2	70.5	70.6	70.5	70.3	69.8	69.6	69.2	68.7	68.1	67.2	66.1
NF [dB]	7.9	6.8	6.1	5.7	5.4	5.0	4.9	4.8	4.6	5.8	4.8	5.1	5.3

Table 10: Voltage gain and noise figure

4.10 Pulling Measurement

The measurement setup is shown in Figure 27.

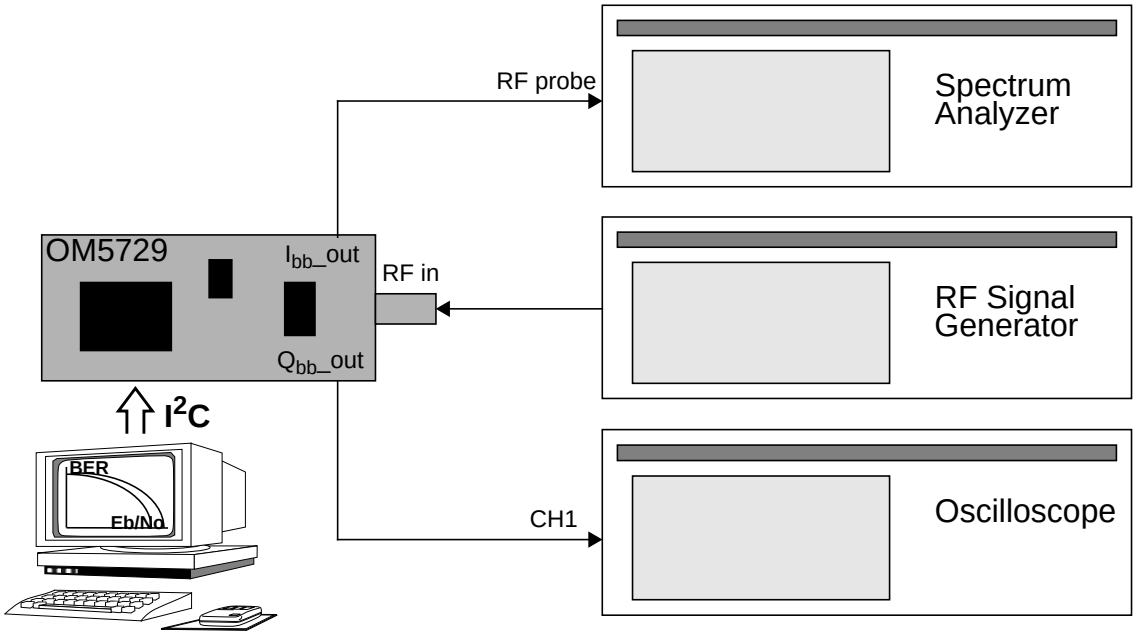


Fig.27 Pulling measurement setup

4.10.1 Measurement procedure

Example:

- Set the RF signal generator to 2151 MHz.
- Set the output level of the sign. gen. to -20 dBm respectively -30 dBm.
- The charge pump current (I_{cp}) setting is set to 120 uA.
- Set the vco frequency to 2150 MHz.
- Send the valid I^2C data once.
- Adjust the AGC voltage at “P11” to 500 mV_{pp} measured in Q $_{baseband\_out}$ with an oscilloscope (CH1).
- Connect a spectrum analyser via a RF probe to the I $_{baseband\_out}$ connector of OM5729.
- Set the spectrum analyser to a START FREQUENCY of 0 kHz, STOP FREQUENCY of 250 kHz, RefLev 0 dBm.
- Set the frequency of the RF signal generator until in baseband an offset of 50kHz is visible (with its harmonics at 100 kHz, 150 kHz, 200 kHz, etc.).
- Measure the distance (level) in baseband between the down-converted signal at 50 kHz and 100 kHz with the spectrum analyser.

4.10.2 Measurement results

In Table 11 and Figure 28, the measurement results are shown:

Freq. [MHz]	950	1050	1150	1250	1350	1450	1550	1650	1750	1850	1950	2050	2150
Pulling level @ -30 dBm [dBc]	-39	-33	-32	-32	-32	-34	-41	-29	-23	-24	-25	-25	-23
Pulling level @ -20 dBm [dBc]	-30	-25	-25	-26	-26	-28	-26	-18	-13	-15	-17	-16	-14

Table 11: Pulling measurement results

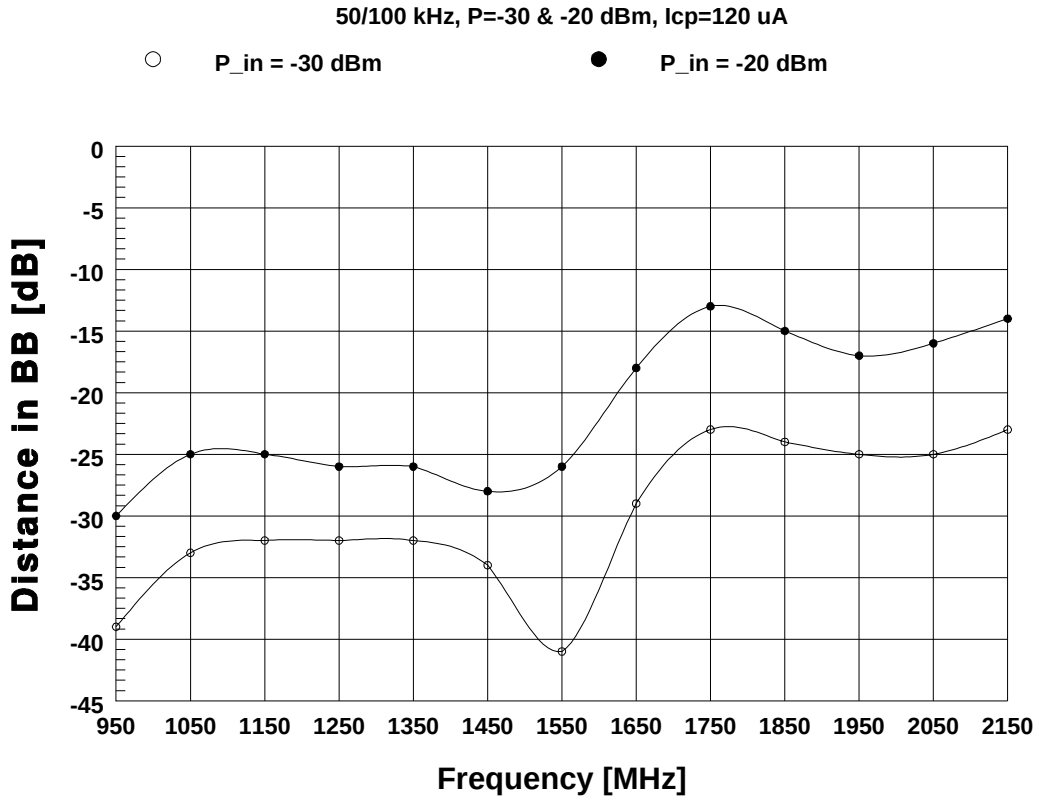


Fig.28 Pulling measurement on OM5729

4.11 BER Measurement

In this paragraph the methods for measuring Bit Error Rates and interpretation of the constellation analyser are discussed. The methods and definitions are only discussed briefly.
For more detailed information see AN99003 - OM5727.

4.11.1 Definition of implementation loss

According to the DVB-S standard the implementation loss must be determined at a BER_{Vit} of $1*10^{-4}$ after the Viterbi decoder according the CANAL+ specification. This will result in a Quasi Error Free MPEG-stream after the Reed-Solomon decoder.

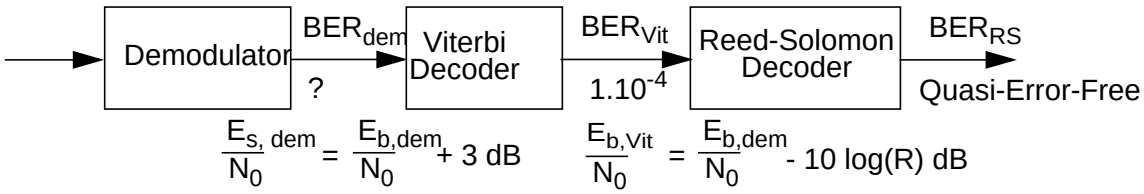


Fig.29 How to determine the implementation loss

4.12 Methods for BER Measurement

Two methods for measuring BER can be distinguished when using the measurement setup of Figure 30.

- BER measurement (after Viterbi) using the Rohde & Schwarz SFQ and the HP3764A signal analyser (BER meter).
- BER measurements (after Demodulator) using the Rohde & Schwarz SFQ and reading out information of the TDA8083 by software.

4.12.1 BER measurement using the BER meter

The SFQ generates a QPSK modulated PRBS stream with Viterbi. This signal is converted to a desired RF frequency within the satellite tuning range. The C/N of the signal can be adjusted on the SFQ. The output of the application board is connected via the measurement interface OM5711 to the BERMETER which measures the BER. This is the BER after Viterbi. The PRBS stream has a length of length 2^{23}-1 and is shaped with a half Nyquist filter.

4.12.2 BER measurement using the DBUI software

The SFQ generates a QPSK modulated PRBS stream with Viterbi. This signal is converted to a desired RF frequency within the satellite tuning range. The C/N of the signal can be adjusted on the SFQ. Using the FNBE I^2C read register the bit error rate can be determined via software. Re-modulation of the Viterbi output results in an internal BER read out option of the BER after the demodulator.

The major disadvantage of this method is that it is not as accurate as the method described in paragraph 4.12.1. The accuracy of this method is depending mainly on the puncturing rate. From measurements can be seen that the software measurement with puncturing rate equal to 1/2 is fairly accurate (within accuracy of noise generation). The software measurements with puncturing rate equal to 7/8 show somewhat less accurate performance, mainly at low signal to noise ratios.

4.13 Optimizing OM5729 for BER Measurements.

- For accurate BER / Implementation Loss measurements, the setup with the SFQ should be calibrated before measuring the BER. If a different symbol rate or a different RF frequency is selected, the SFQ should be calibrated again. The calibration method is described in the application note of R&S called: *"Bit Error Ratio BER in DVB as a function of C/N"*.
- The BER measurement can gibe better results by optimizing the fixed gain setting for the coarse AGC with the software while looking at the number of errors. The nominal level for I and Q at the tuner output should be 0.8 V_{pp}.
- For all symbol rates it is desirable to switch off the I^2C bus to the tuner to avoid cycle slips when the system is locked.

The performance of the OM5729 Zero-IF demo board in combination with the TDA8083 SDD IC depends on several factors. The main factors are:

- Loop settings of the TDA8083
- Tuner properties like phase noise, pass-band flatness, tilt and phase behaviour
- The used symbol rate

For high symbol rates especially the Tuner properties low pass filter flatness and phase play an important role. For lower symbol rates, the phase noise behaviour of the tuner is critical.

4.13.1 BER measurement setup

In Figure 30 the measurement set up is given used for the evaluation of the OM5729 demo board in combination with the measurement interface OM5711/M/C2.

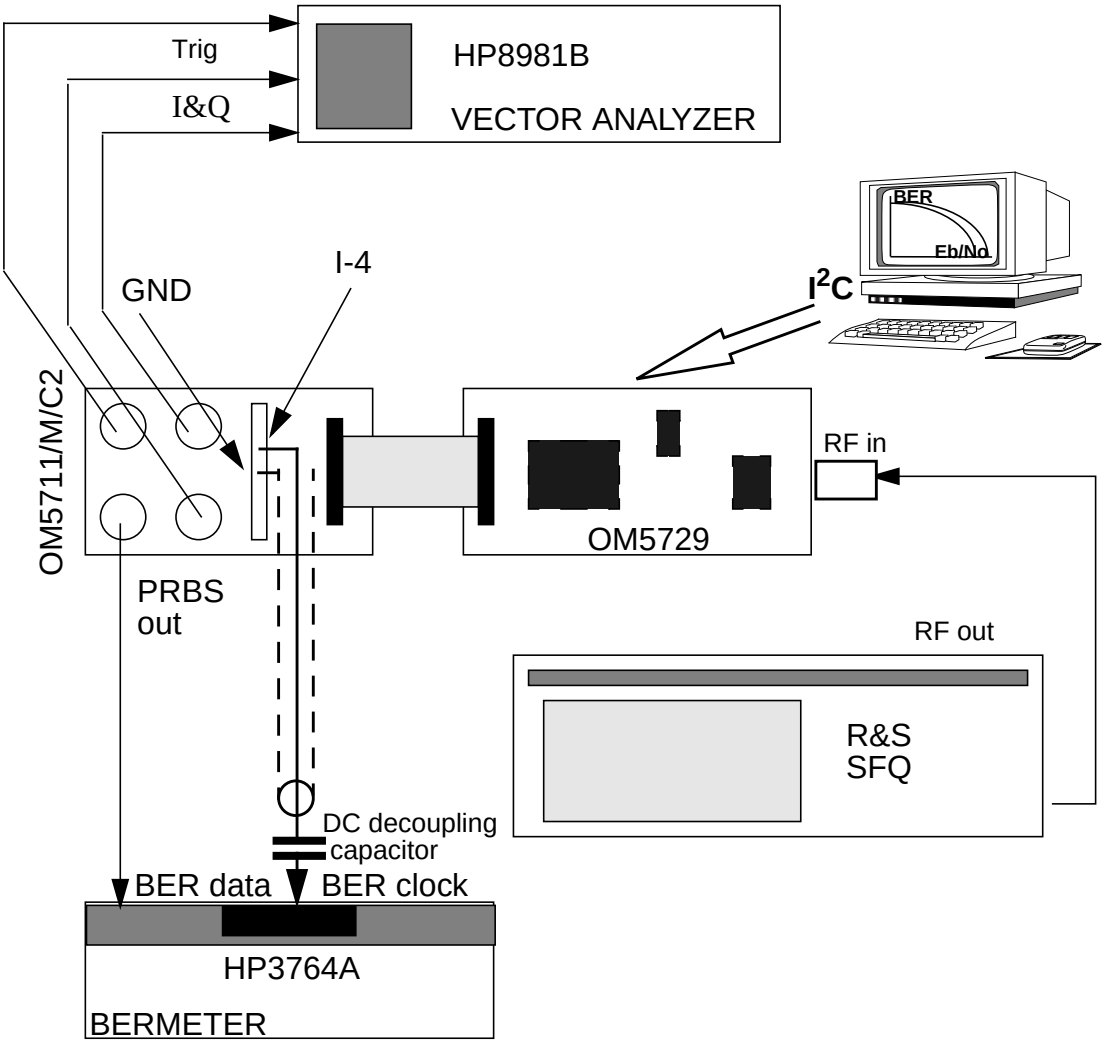


Fig.30 BER Measurement setup

4.14 C/N as function of Input Power Level

This measurement can be used to see at which QPSK modulated RF input power level (at different frequencies and symbol rates) the BER value degrades or even cycle slips occur.
In the application note of R&S the relationship can be found between C/N (used by SFQ) and E_b/N_{o_vit}, as used by Canal+:

$$\frac{E_{b,vit}}{N_0} = \frac{C}{N} \text{ - 3 dB - 10 log(R) dB + 10 log (1-0.25a)}$$

with R = puncturing rate (e.g. 5/6) and a = roll off factor (e.g. 0.35). Since we do not use Reed Solomon in our measurement, this formula does not take the Reed Solomon correction factor into account: - 10 log (188/204)

Note: Errors due to measurement setup equipment are not taken into account. Therefore these measurement results are for comparative use only.

4.14.1 Hardware settings of the OM5729

- At the top side of the board, close solder jumper “J103”.
- At the top side of the board, close solder jumper “J100” & “J101”.
- At the bottom side of the board, close solder jumper “J104”.
- At the top side of the board, set jumper “J1” to automatic AGC.
- If present, remove resistors “R15” and “R36” (10 kOhm).
- Connect the power supplies of the OM5729:
  - Connect “P2” to +5 V.
  - Connect “P3” to GND.
  - Connect “P8” to GND.
  - Connect “P6” to +28 V.
  - Connect “P101” (GND) to GND.
  - Connect “P102” to +3.3 V.
  - Connect “P103” (GND) to GND.
  - Connect “P1” (+5 V_d) to +5 V.
- Do not connect any probes to the I and the Q output during BER measurement, since this will influence the measurement result.

4.14.2 Hardware settings of the OM5711/M/C2

- The BER clock needed for the BER meter is now derived from the i-4 pin of connector “P2” on the measurement interface OM5711/M/C2 instead of BNC connector “P7”.
  A capacitor is required to prevent incorrect operation of the BER meter.
  The capacitor value should be about 10 uF. See also Figure 30.

4.14.3 Software settings of the OM5729

- Connect the I^2C bus connector of the demo board to an I^2C interface board.
- Start the DBUI software.
- Select the correct frequency related settings.
- Select the desired puncturing rate in the FEC menu. Only one puncturing rate should be selected as the FEC is not able to automatically select the correct puncturing rate in this test mode.
- Select the “No Spectral Inversion”.
- Select in the main menu test mode “C” for Viterbi output measurements.
- Push the “Preset” button in the software until the BER meter is locked.
- Always Disable the “I^2C tuner” setting after a change of settings, before measuring.

4.14.4 Settings of the SFQ

The Rohde & Schwarz SFQ is used to generate the Viterbi encoded PRBS QPSK signal. The Viterbi encoded PRBS QPSK signal is required for implementation margin (IM), also referred to as implementation loss (IL), measurements as described in the CANAL+ specification document.
To be able to measure BER after Viterbi, a number of changes have to be made from the original setup (see application note om5719 - AN89049) and software configuration, which are discussed step-by-step.

Let's assume a setup with a symbol rate (S.R.) of 27.5 MS/s and the puncturing rate (P) is 5/6.
For other configurations, change the settings of the SFQ and the software accordingly.

SFQ settings:

INPUT:	TS parallel
PACKET LENGHT:	188 byte
MODE:	PRBS
ROLL-OFF:	0.35
RATE:	5/6
SPECIAL:	Scrambling off, Interleaving off, RS off
SYMBOL RATE:	27.5 MS/s
C/N:	Adjust and read-out BER value (1e-4)
NOISE BW:	27.5 MHz (set always to the same value as Symbol Rate)
NOISE:	On

4.14.5 Measurement procedure

After the hardware, the software and the SFQ have been setup with a specified symbol rate (S.R.), puncturing rate (P) and RF frequency (f), adjust at different QPSK modulated RF input power levels the C/N value of the SFQ until the BER meter reads 1e-4. The value 1e-4 is referring to the CANAL+ specification. A lower C/N value required at a certain input level means a better system performance. There is a linear relationship between the C/N value and the implementation margin value: 0.1 dB more C/N represents 0.1dB more implementation margin.

- "*Pin"* represents the QPSK modulated RF input power level of the SFQ.
- *"C/N"* represents the setting of the C/N value of the SFQ where the BER value is 1e-4.
- *"c.s."* represents the input power level where cycle slips occur frequently. To obtain this value, the noise option of the SFQ is switched OFF.
- *"a"* represents the roll off factor of the QPSK modulated spectrum (e.g.: a = 0.35).

4.14.5.1 measurement with 27.5 MS/s and P = 5/6

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	9.4	8.4	8.0	7.9	7.9	7.9	7.9	7.9	7.9	8.1	8.4	8.6	c.s.		

Table 12: f=950 MHz, S.R.=27.5 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	8.4	8.0	7.9	7.9	7.9	7.9	7.9	7.9	8.0	8.1	8.6	c.s.			

Table 13: f=1350 MHz, S.R.=27.5 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	8.3	8.0	7.9	7.9	7.9	7.9	7.9	7.9	8.0	8.1	8.5	9.0	c.s.		

Table 14: f=1500 MHz, S.R.=27.5 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	8.4	8.0	7.9	7.9	7.9	7.9	7.9	7.9	8.1	8.3	8.8	c.s.			

Table 15: f=2150 MHz, S.R.=27.5 MS/s, P=5/6, a=0.35

4.14.5.2 measurement with 27.5 MS/s and P = 3/4

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.9	7.3	6.9	6.9	6.8	6.8	6.8	6.8	6.8	7.0	7.2	7.5	7.6	7.7	c.s.

Table 16: f=950 MHz, S.R.=27.5 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.2	7.0	6.9	6.8	6.8	6.8	6.8	6.8	6.8	7.1	7.5	c.s.			

Table 17: f=1350 MHz, S.R.=27.5 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.1	6.9	6.8	6.8	6.8	6.8	6.8	6.8	6.8	7.1	7.4	7.9	c.s.		

Table 18: f=1500 MHz, S.R.=27.5 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.2	6.9	6.9	6.8	6.8	6.8	6.8	6.8	6.9	7.2	c.s.				

Table 19: f=2150 MHz, S.R.=27.5 MS/s, P=3/4, a=0.35

4.14.5.3 measurement with 27.5 MS/s and P = 1/2

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.5	4.2	4.0	4.0	4.0	4.0	4.0	4.0	4.1	4.2	4.4	4.6	4.9	5.0	c.s.

Table 20: f=950 MHz, S.R.=27.5 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.2	4.1	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.3	c.s.				

Table 21: f=1350 MHz, S.R.=27.5 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.1	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.2	4.6	c.s.			

Table 22: f=1500 MHz, S.R.=27.5 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.2	4.1	4.0	4.0	4.0	4.0	4.0	4.0	4.2	c.s.					

Table 23: f=2150 MHz, S.R.=27.5 MS/s, P=1/2, a=0.35

4.14.5.4 measurement with 15.0 MS/s and P = 5/6

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	8.5	7.9	7.8	7.7	7.7	7.7	7.7	7.7	7.7	7.8	8.0	8.1	8.2	8.4	c.s.

Table 24: f=950 MHz, S.R.=15.0 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.9	7.8	7.7	7.7	7.7	7.7	7.7	7.7	7.8	7.9	c.s.				

Table 25: f=1350 MHz, S.R.=15.0 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.9	7.8	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	8.1	8.9	c.s.		

Table 26: f=1500 MHz, S.R.=15.0 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	8.0	7.8	7.7	7.7	7.7	7.7	7.7	7.8	7.9	8.7	c.s.				

Table 27: f=2150 MHz, S.R.=15.0 MS/s, P=5/6, a=0.35

4.14.5.5 measurement with 15.0 MS/s and P = 3/4

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.6	7.1	7.0	6.9	6.9	6.8	6.9	6.9	6.9	7.0	7.1	7.2	7.3	7.3	c.s.

Table 28: f=950 MHz, S.R.=15.0 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.0	6.9	6.9	6.9	6.9	6.9	6.9	6.9	6.9	7.0	c.s.				

Table 29: f=1350 MHz, S.R.=15.0 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.0	6.9	6.9	6.9	6.9	6.9	6.9	6.9	6.9	7.0	7.3	8.0	c.s.		

Table 30: f=1500 MHz, S.R.=15.0 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.0	6.9	6.9	6.9	6.9	6.9	6.9	6.9	7.0	c.s.					

Table 31: f=2150 MHz, S.R.=15.0 MS/s, P=3/4, a=0.35

4.14.5.6 measurement with 15.0 MS/s and P = 1/2

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.2	4.0	4.0	3.9	3.9	3.9	3.9	3.9	c.s.						

Table 32: f=950 MHz, S.R.=15.0 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.0	4.0	3.9	3.9	3.9	3.9	3.9	3.9	4.0	c.s.					

Table 33: f=1350 MHz, S.R.=15.0 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.0	4.0	3.9	3.9	3.9	3.9	3.9	3.9	4.0	4.1	c.s.				

Table 34: f=1500 MHz, S.R.=15.0 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.0	4.0	3.9	3.9	3.9	3.9	3.9	4.0	c.s.						

Table 35: f=2150 MHz, S.R.=15.0 MS/s, P=1/2, a=0.35

4.14.5.7 measurement with 12.0 MS/s and P = 5/6

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	8.5	7.9	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	8.0	8.1	8.1	8.1	8.1

Table 36: f=950 MHz, S.R.=12.0 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.8	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.9	c.s.				

Table 37: f=1350 MHz, S.R.=12.0 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.8	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.7	7.8	8.2	c.s.			

Table 38: f=1500 MHz, S.R.=12.0 MS/s, P=5/6, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.9	7.7	7.7	7.7	7.7	7.7	7.7	7.8	8.0	c.s.					

Table 39: f=2150 MHz, S.R.=12.0 MS/s, P=5/6, a=0.35

4.14.5.8 measurement with 12.0 MS/s and P = 3/4

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	7.3	6.9	6.7	6.6	6.6	6.6	6.6	6.6	6.7	6.7	7.0	7.1	7.1	7.2	c.s.

Table 40: f=950 MHz, S.R.=12.0 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	6.7	6.7	6.6	6.6	6.6	6.6	6.6	6.6	6.7	6.9	c.s.				

Table 41: f=1350 MHz, S.R.=12.0 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	6.7	6.7	6.6	6.6	6.6	6.6	6.6	6.6	6.7	6.8	7.1	8.0	c.s.		

Table 42: f=1500 MHz, S.R.=12.0 MS/s, P=3/4, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	6.8	6.6	6.6	6.6	6.6	6.6	6.6	6.7	6.9	c.s.					

Table 43: f=2150 MHz, S.R.=12.0 MS/s, P=3/4, a=0.35

4.14.5.9 measurement with 12.0 MS/s and P = 1/2

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]		4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.1	c.s.				

Table 44: f=950 MHz, S.R.=12.0 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.1	c.s.					

Table 45: f=1350 MHz, S.R.=12.0 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.2	c.s.				

Table 46: f=1500 MHz, S.R.=12.0 MS/s, P=1/2, a=0.35

Pin [dBm]	-75	-70	-65	-60	-50	-40	-30	-25	-20	-15	-10	-5	0	+5	+10
C/N [dB]	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.1	c.s.						

Table 47: f=2150 MHz, S.R.=12.0 MS/s, P=1/2, a=0.35

APPENDIX 1 Board interfaces and functions

Switches and Jumpers

Table 48: Overview jumpers and switches

Function	Switch / jumper	Comments	On delivery of board:
I and Q from tuner part	“J100” and “J101” closed	On PR39233 board	jumpers closed
+5 V_a to SDD (AGC)	“J103” closed	If “J103” closed, don’t use “P100”	jumper closed
AGC select	“J1”	Manual or automatic AGC	AGC automatic
BER_I or BER_Q	Switch “S1”	On OM5711/M/C2 board	-

Input and Output overview

The following connector and test pins are available on the application board:

Table 49: Overview of application board connectors and test pins

Function	Connector type	I/O	Imped. (Ohm)	Level	Comments
OM5729					
L-band tuner input	One SMA-connector	I	50	-25 to -65 dBm	
I&Q analogue output	Test pins “P10” and “P13”	O	10k	0.5 .. 0.8 V_{pp}	
MPEG2 packet stream output	26 Pole Male IDC, P1100	I/O		0 .. 3.3 V	TTL levels, includes I^2C and interrupt
V_{agc}	test pin “P107”	O	470	0.5 .. 4.5 V	Signal from PWM output
OM5711/M2 measurement interface board					
PRBS_out	BNC, “P6”	O	75		To transmission analyser, AC coupled
I&Q sampled	BNC (2x), “P1” and “P2”	O	50	0.5 V_{pp}	To constellation analyser, AC coupled
clock_out	BNC, “P7”	O	50	TTL	AC coupled
I&Q digital, sampled	16 pins “P2” and “P5”	O	high	0 .. 3.3 V	TTL levels, for logic analyser
Supply	pins and wires	I			5 V, 3.3 V, 28 V
I^2C	4 pin Stocko	I/O		0 .. 5 V	pull-up 10k on board

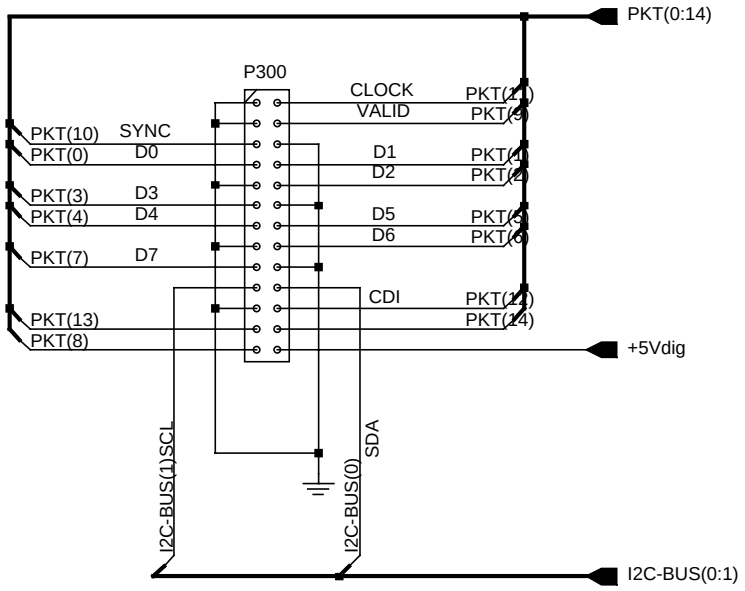
MPEG2 TTL output

This interface is meant for inter-board connection (at short distances). Besides the MPEG2 inputs it provides I^2C, valid flags and interrupt pin, see Table 50. The TDA8083 I^2C, AGC and interrupt line are 5 V compatible.

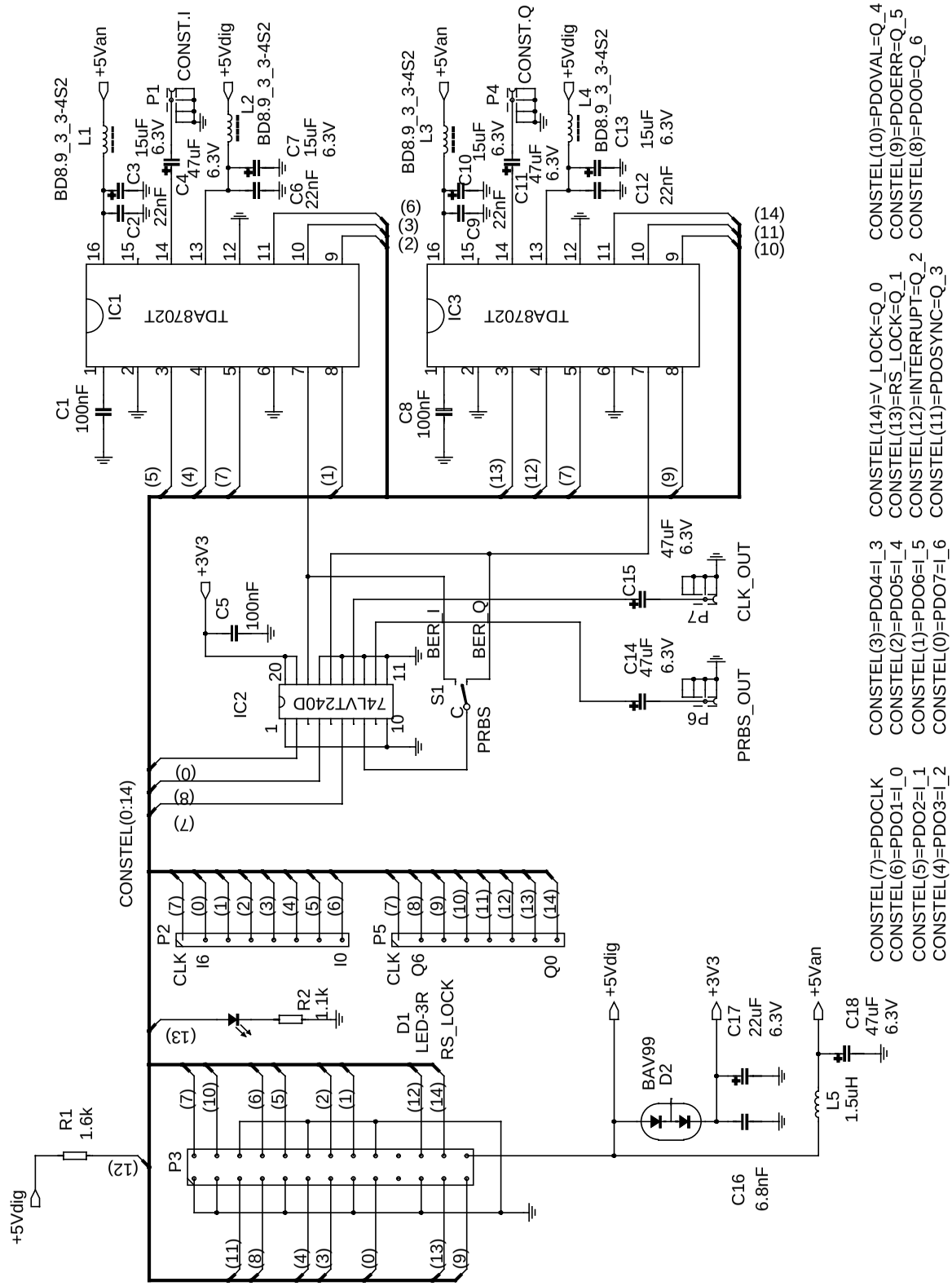
Connector type: A 26 Pole Male IDC connector is used.

Table 50: Pin assignment of the MPEG2 TLL interface

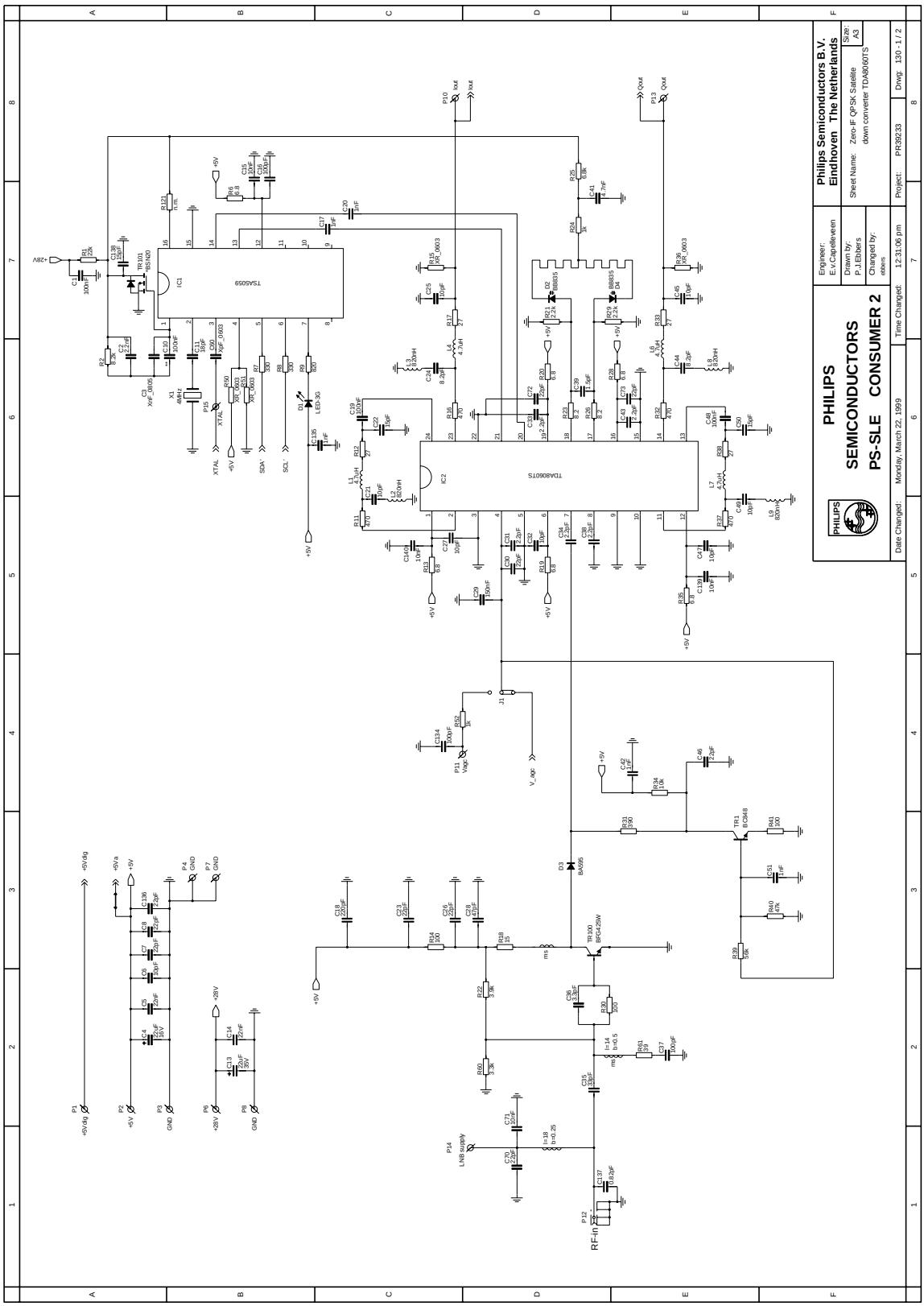
IC pin Name	I/O	Description	Pin Position
PDO0	I	MPEG output Data 0	7
PDO1	I	MPEG output Data 1	8
PDO2	I	MPEG output Data 2	10
PDO3	O	MPEG output Data 3	11
PDO4	O	MPEG output Data 4	13
PDO5	O	MPEG output Data 5	14
PDO6	O	MPEG output Data 6	16
PDO7	O	MPEG output Data 7	17
PDOCLK	O	MPEG output Clock	2
PDOSYNC	O	MPEG Sync output	5
PDOVAL	O	MPEG Valid output	4
INT	O	Channel Decoder Interrupt	22
PDOERR	O	Transport error indicator	25
SCL	O	I^2C Clock	19
SDA	I/O	I^2C Data	20
VLOCK	O	Viterbi Lock indicator	24
RSLOCK	O	RS Lock indicator	23
Vss		Digital Ground	1,3,6,9,12,15,18,21,
+5 V		+5 V (Supply)	26

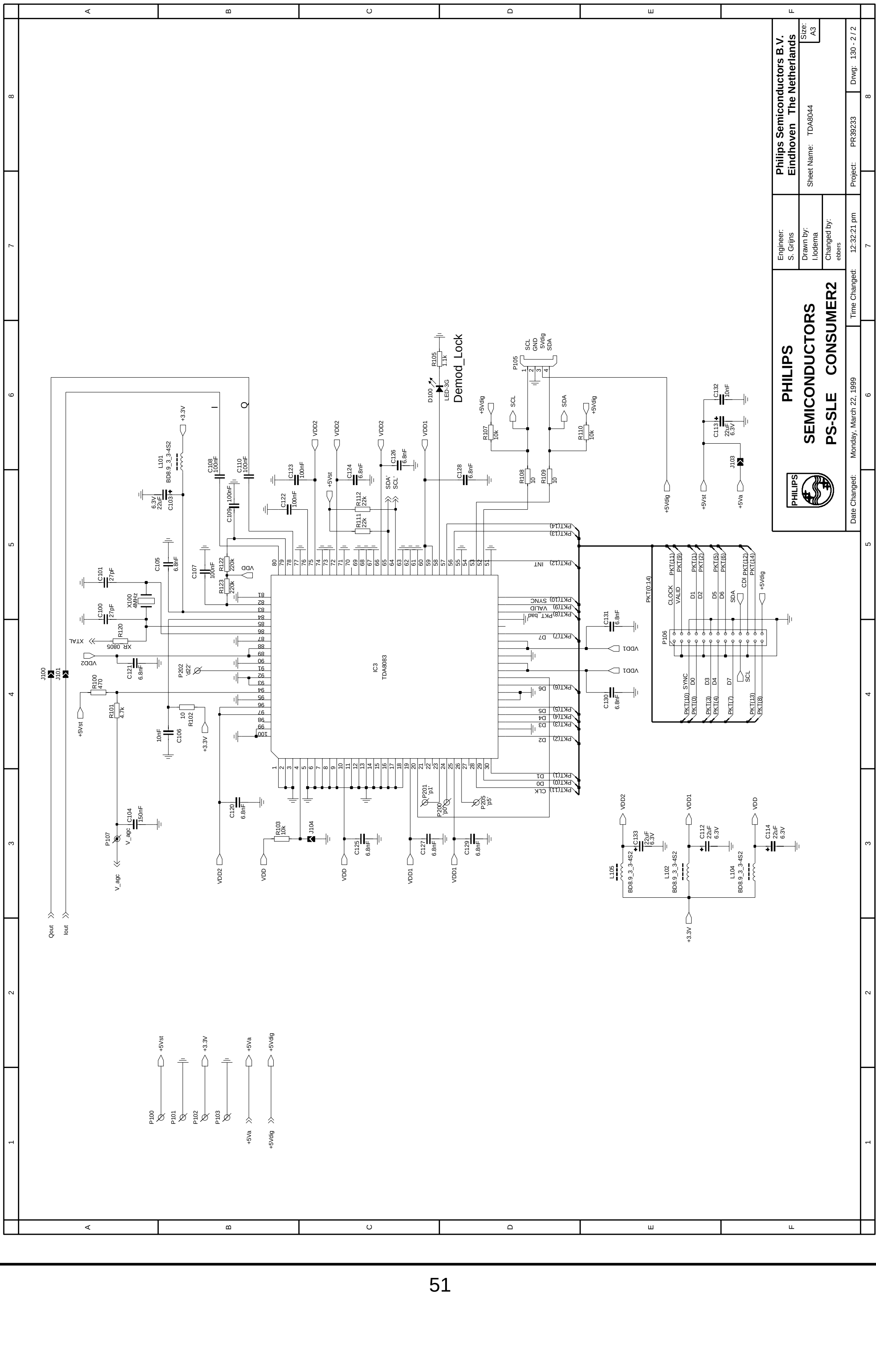


APPENDIX 2 Schematic of the measurement interface board OM5711/M2



APPENDIX 3 Board schematics of OM5729




Philips Semiconductors B.V.
Eindhoven The Netherlands
Sheet Name: TDA8044
Project: PR39233
Drwg: 130 - 2 / 2
Size: A3
Engineer: S. Grijns
Drawn by: I.Iodema
Changed by: ebbers
PHILIPS
SEMICONDUCTORS
PS-SLE CONSUMER2
Date Changed: Monday, March 22, 1999
Time Changed: 12:32:21 pm
IC3
TDA8083
Demod_Lock

APPENDIX 4 Board layout of OM5729

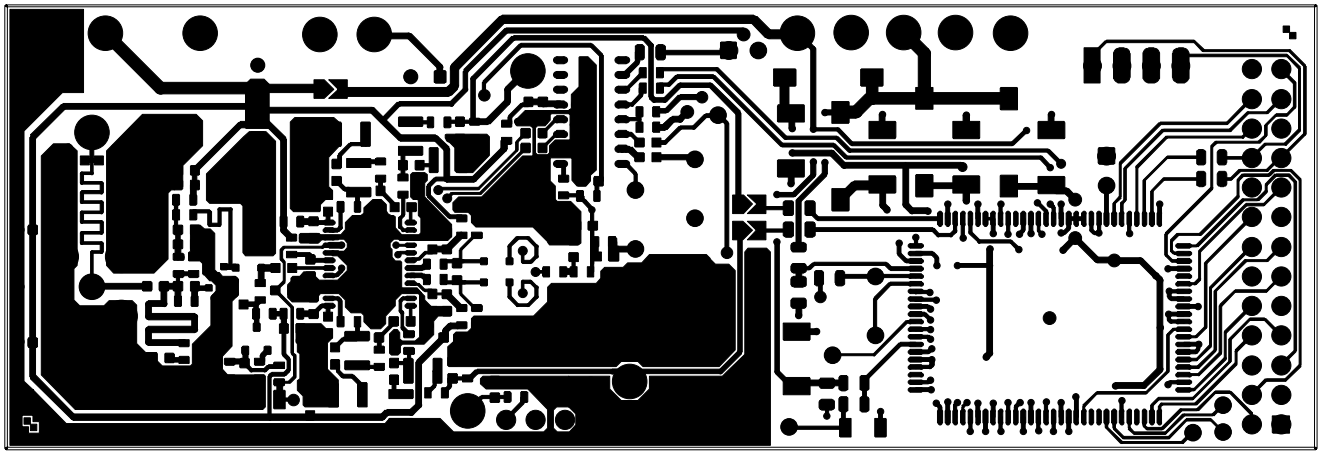


Fig.31 Top side of the pcb

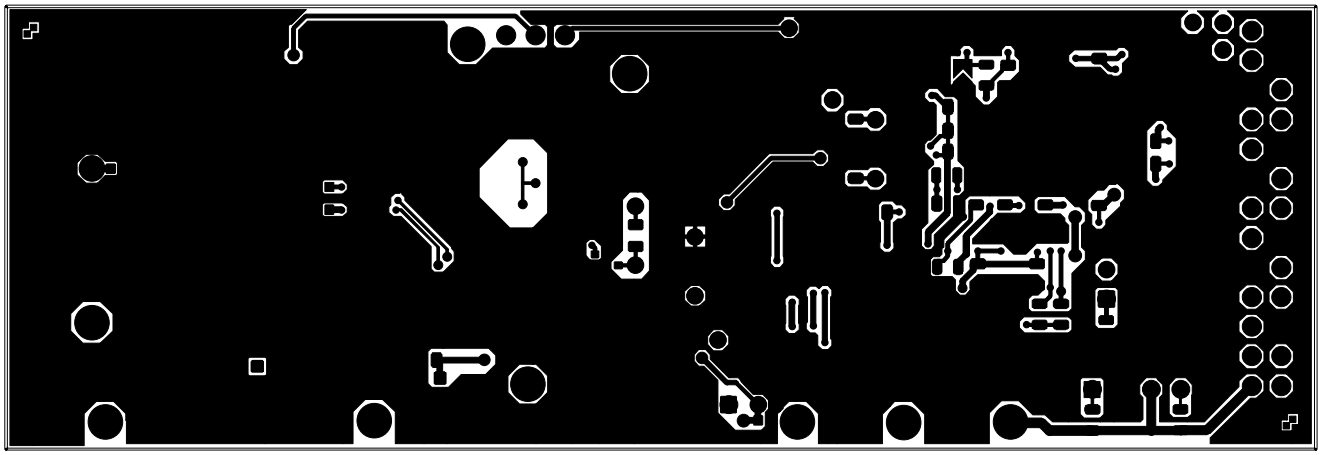


Fig.32 Bottom side of the pcb

APPENDIX 5 Bill of materials of project OM5729

ITEM	CNT	COMPONENT	SERIES	TOL.	RATING	VENDOR	GEOMETRY	REFERENCE
1	1	BOARD PR39233				PS-SLE	BOARD	
2	3	100nF	X7R	20%	16V	PHILIPS	C0603	C1 C19 C48
3	1	3.9nF	MKT 370	10%	250V	PHILIPS	C370_A	C10
4	2	27pF	NP0	5%	50V	PHILIPS	C0805	C100 C101
5	5	22uF	B45196	20%	6.3V	SIEMENS	B45_c	C103 C112 C113 C114 C133
6	11	6.8nF	X7R	10%	50V	PHILIPS	C0805	C105 C120 C121 C124 C125 C126 C127 C128 C129 C130 C131
7	2	10nF	X7R	10%	50V	PHILIPS	C0805	C106 C132
8	4	100nF		20%	50V	PHILIPS	C0805	C107 C108 C109 C110
9	1	18pF	NP0	5%	50V	PHILIPS	C0603	C11
10	2	100nF	X7R	20%	50V	PHILIPS	C0805	C122 C123
11	1	22uF	RLP5 134	20%	35V	PHILIPS	CASE_R55_CA	C13
12	1	0.82pF	NP0	0.25pF	50V	PHILIPS	C0603	C137
13	1	JUMPER_CAP				PHILIPS	JUMPER_3p	J1
14	4	10nF	X7R	20%	25V	PHILIPS	C0603	C15 C71 C139 C140
15	3	100pF	NP0	5%	50V	PHILIPS	C0603	C16 C37 C134
16	5	1nF	X7R	10%	50V	PHILIPS	C0603	C17 C20 C42 C51 C135
17	1	220pF	X7R	10%	50V	PHILIPS	C0603	C18
18	1	82pF	NP0	5%	50V	PHILIPS	C0603	C2
19	3	15pF	NP0	5%	50V	PHILIPS	C0603	C22 C50 C138
20	2	8.2pF	NP0	0.5pF	50V	PHILIPS	C0603	C24 C44
21	1	47pF	NP0	5%	50V	PHILIPS	C0603	C28
22	2	150nF	X7R	10%	25V	PHILIPS	C1206	C29 C104
23	1	XnF_0805	C0805-X7R	10%	63V	PHILIPS	C0805	C3
24	5	2.2pF	NP0	0.25pF	50V	PHILIPS	C0603	C31 C33 C34 C38 C43
25	1	33pF	NP0	5%	50V	PHILIPS	C0603	C35
26	1	3.3pF	NP0	0.25pF	50V	PHILIPS	C0603	C36
27	1	1.5pF	NP0	0.25pF	50V	PHILIPS	C0603	C39
28	1	22uF	RLP5 134	20%	16V	PHILIPS	CASE_R54_CA	C4
29	1	1.5nF	X7R	10%	50V	PHILIPS	C0603	C41
30	2	22nF	X7R	10%	50V	PHILIPS	C0805	C5 C14
31	8	10pF	NP0	5%	50V	PHILIPS	C0603	C6 C21 C25 C27 C32 C45 C47 C49
32	1	XpF_0603	C0603-X7R	10%	63V	PHILIPS	C0603	C60
33	10	22pF	NP0	5%	50V	PHILIPS	C0603	C7 C8 C23 C26 C30 C46 C70 C72 C73 C136
34	2	LED-3G	Low_Cost			TEXIM	SOD53	D1 D100
35	2	BB835	VaricapDiode			SIEMENS	SOD323	D2 D4
36	1	BA595	Pin_diode			SIEMENS	SOD323	D3
37	1	TSA5059T	IC_RF_Synth			PHILIPS	SOT109	IC1
38	1	TDA8060TS	IC_ZIF_Downc			PHILIPS	SOT340	IC2
39	1	TDA8083H	IC_SDD			PHILIPS	SOT317	IC3

40	1	JUMPER_3p	print_switch			PHILIPS	JUMPER_3p	J1
41	4	4.7uH	FSLU2520	5%		TOKO		L1 L4 L6 L7
42	4	BD8.9_3_3-4S2	CBD			PHILIPS	CBD8.9	L101 L102 L104 L105
43	4	820nH	FSLU2520	5%		TOKO		L2 L3 L8 L9
44	15	SOLD-PIN_large				PHILIPS		P1 P2 P3 P4 P6 P7
								P8 P10 P11 P13 P14
								P100 P101 P102 P103
45	1	MKS3730_4p	MKS3730			STOCKO	MKS3730_4p	P105
46	1	ARRAY_2x13p	DOUBLE_ARRAY			DISPLAY	ARRAY_2x13p	P106
47	1	SMA_SCREW_sqr	COAX			RADIALL	SMA_sqr	P12
48	6	SOLD-PIN_small				PHILIPS		P15 P107 P200 P201
								P202 P205
49	1	22k	RC21	5%	0.063W	PHILIPS	R0603	R1
50	1	470	RC11	5%	0.1W	PHILIPS	R0805	R100
51	1	4.7k	RC11	5%	0.1W	PHILIPS	R0805	R101
52	3	10	RC11	5%	0.1W	PHILIPS	R0805	R102 R108 R109
53	3	10k	RC11	5%	0.1W	PHILIPS	R0805	R103 R107 R110
54	1	1.1k	RC11	5%	0.1W	PHILIPS	R0805	R105
55	4	470	RC21	5%	0.063W	PHILIPS	R0603	R11 R16 R32 R37
56	2	22k	RC11	5%	0.1W	PHILIPS	R0805	R111 R112
57	4	27	RC21	5%	0.063W	PHILIPS	R0603	R12 R17 R33 R38
58	1	XR_0805	RC11	1%	0.1W	PHILIPS	R0805	R120
59	1	0	RC21	5%	0.063W	PHILIPS	R0603	R121
60	2	220k	RC11	5%	0.1W	PHILIPS	R0805	R122 R123
61	3	100	RC21	5%	0.063W	PHILIPS	R0603	R14 R30 R41
62	4	XR_0603	RC11	1%	0.1W	PHILIPS	R0603	R15 R36 R50 R51
63	1	15	RC21	5%	0.063W	PHILIPS	R0603	R18
64	1	27k	RC21	5%	0.063W	PHILIPS	R0603	R2
65	2	2.2k	RC21	5%	0.063W	PHILIPS	R0603	R21 R29
66	1	3.9k	RC21	5%	0.063W	PHILIPS	R0603	R22
67	2	8.2	RC21	5%	0.063W	PHILIPS	R0603	R23 R26
68	2	1k	RC21	5%	0.063W	PHILIPS	R0603	R24 R52
69	1	2.7k	RC21	5%	0.063W	PHILIPS	R0603	R25
70	1	390	RC21	5%	0.063W	PHILIPS	R0603	R31
71	1	10k	RC21	5%	0.063W	PHILIPS	R0603	R34
72	1	56k	RC21	5%	0.063W	PHILIPS	R0603	R39
73	1	47k	RC21	5%	0.063W	PHILIPS	R0603	R40
74	6	6.8	RC21	5%	0.063W	PHILIPS	R0603	R6 R13 R19 R20 R28
								R35
75	1	3.3k	RC21	5%	0.063W	PHILIPS	R0603	R60
76	1	39	RC21	5%	0.063W	PHILIPS	R0603	R61
77	2	330	RC21	5%	0.063W	PHILIPS	R0603	R7 R8
78	1	820	RC11	5%	0.1W	PHILIPS	R0805	R9
79	1	BC848	Gen_Purpose			PHILIPS	SOT23	TR1
80	1	BFG425W	BroadBand			PHILIPS	SOT343R	TR100
81	1	BSN20	NMOS fets			PHILIPS	SOT23	TR101
82	2	4MHz	Crystal			PHILIPS	HC49_u13	X1 X100